Learning Electronics – The Empirical Approach

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Preface

Electronics is a common platform supporting technological advances that continuously reshape the society. Core courses of circuits in the electrical engineering curriculum are partioned into circuit analysis, electronics and technical electives involving advanced circuits for specific applications. The purpose of this manuscript is to provide an overall view from passive components, semiconductor devises, electronic circuits to applications. Of course, one manuscript cannot cover everything in details. Only essential concepts, devices and circuits with subsequent implications are discussed.

Textbooks focus on theoretical analyses. There are many equations. To concur with the theory, laboratory manuals focus on procedures and results. The empirical approach is a unique way to learn electronics. Different from textbooks, only few essential equations are introduced. While following the manuscript, readers may feel like carrying out virtual or real experiments. However, the emphasis is not on getting specific results. The emphasis is on correlations between causes and consequences as well as observations and understandings. In other words, readers engage in active and experiential leaning. After gaining the crucial knowledge and experiences, readers can design and optimize new electronic circuits.

There are five sections in the manuscript. Chapters 1-4 review the essential background information. Chapters 5-8 discuss the building blocks of electronic circuits. Chapters 9-11 present digital and interface circuits. Chapters 12-15 focus on advanced analog circuits. The remaining chapters discuss application circuits.

To facilitate the experiential learning, readers can use a circuit simulation program or a personal instrument module. For those who choose simulations, you need to download, install, and customize LTspice, a free circuit simulation program. If practicing virtual circuit construction is desired, readers can download and install one breadboard emulation program, such as Fritzing, Virtual Breadboard or Pebble, discussed in Appendix B.

Those who wish to implement circuits and perform measurements need to acquire a personal instrument module, either Digilent Analog Discovery 2 or Analog Devices ADALM2000. Please read Appendix C. Readers also need to acquire the Analog Parts Kit ADALP2000 and the following semiconductor components: two 74HC00, one 74HC14, two 74HC74, one 74HC86, one LM317, five additional 2N3904 BJT, one 2N3819 JFET, one CD4007 and one CD4046. Having spare semiconductor devices and passive component kits of resistors, capacitors, inductors are very useful.

1. Fundamental Electricity and Magnetism

In this chapter, we review fundamental concepts in electricity and magnetism critical to electronics. We will focus only on essential knowledge which are needed in subsequent chapters.

Charged particles play the key role in electricity and electronics. Electrons, which are negatively charged, transport electricity in the metallic power grid. Electronic devices control the flow of electrons and positively charged holes in semiconductors. By separating and accumulating charges of opposite polarity, an electrical potential, i.e., voltage, is generated. The flow of charge leads to current. Charge, Q, is measured in Coulomb (C); voltage, V, in Volt (V); and current, I, in Ampere (A). To represent quantities of different magnitudes, a prefix is added, e.g., milli (m) for 10^{-3}, micro (μ) for 10^{-6}, nano (n) for 10^{-9}; pico (p) for 10^{-12}; likewise, kilo (k) for 10^{3}, mega (M) for 10^{6}, giga (G) for 10^{9} and tera for 10^{12}.

Constant, non-time-varying current is called direct current (dc). Signal, which varies through positive and negative values over time, is called alternating current (ac). The average or integration of an ac signal over a long span of time is zero. Power supply for electronics is dc. Electricity distributed by the power grid is ac. Electronic signals often carry both dc and ac components. For simplicity, we will use capital letters for all variables. They can be implicitly time dependent. For example, the rate of change or time differentiation of charge is current:

$$I(t) = \frac{dQ(t)}{dt}. \tag{1}$$

Each electron carries a negative charge of $1.6\text{x}10^{-19}$ Coulomb. What is the number of electrons passing by per nsec in a wire carrying a 1-mA current? (Answer: $6.25\text{x}10^{6}$.) For a given voltage, resistor controls the current according to the Ohm's law:

$$I(t) = \frac{V(t)}{R}. \tag{2}$$

We, as human, can feel electrical shock with a 1-mA current. The resistance of the body is of the order of 100 kΩ. The 120-V ac outlet on the wall can and will cause electrical shock. When the skin is wet, its resistance drops down to 10 kΩ making the electrical shock hazard very serious. A current above 10 mA can cause muscle paralysis making the victim unable to retreat from the electrical source. It becomes lethal when the current reaches 100 mA.

Charge multiplied by voltage is energy, $\mathcal{E}$, in unit of Joule (J). Power, P, measured in Watt (W), is the rate of change or time differentiation of energy. Resistors consume power according to:

$$P(t) = I^2(t)R = I(t) \cdot V(t) = \frac{V^2(t)}{R}. \tag{3}$$

The central processing unit (cpu) of a notebook computer operates with a voltage of 0.7 V and consumes 15 W. What is its current? (Answer: 21.4 A.) Although you can use any resistance in circuit simulations, real resistors have limited power handling capabilities. Operating above its power rating, a resistor can and will burn. Most resistors used in electronic circuits can only handle one-quarter Watt, 250 mW, or one-eighth Watt. The resistance of an inline resistor is marked by color bands. Black, brown, red, orange, yellow, green, blue, purple, gray and white represent numerical values, 0-9, respectively. For carbon film resistors, the first and second color bands represent the first and second significant digits. The third color band represents the multiplication factor. For example, red represents a multiplication factor of 10^2. Therefore, a carbon film resistor with brown green red color bands has a resistance of 15×10^2 Ω, i.e., 1.5 kΩ. The fourth color band represents the tolerance. Gold represents 5% tolerance and silver 10%. For high precision metal film resistors, there are up to seven bands. The first three bands represent three significant digits. The fourth band is the multiplication factor. In addition to colors representing 0-9, gold multiplication factor represents x0.1 and silver represents x0.01. The fifth band represents the tolerance. The sixth band represents the temperature coefficient and the seventh band represents the reliability. Modern electronic systems, such as cellular phones, use small, surface-mount resistors. Their resistances are marked by numbers, for example, 102 represents $10\text{x}10^2$ or 1 kΩ.

Capacitor is formed by sandwiching a dielectric medium between two electrodes. Voltage is given by the ratio of charge and capacitance. Charge accumulates via the flow of current through a capacitor.

$$V(t) = \frac{Q(t)}{C} = \frac{1}{C}\int I(t) \cdot dt. \tag{4}$$

As a result of integration, the voltage and current of a capacitor are not synchronized. The voltage may reach its peak value later than the current. The energy stored in a capacitor gradually builds up from zero as the capacitor charges up. When the capacitor is fully charged, the energy stored is given by

$$\mathcal{E} = \int_0^Q \frac{Q}{C} dQ = \frac{Q^2}{2C} = \frac{CV^2}{2} \tag{5}$$

A photoflash operates with a capacitance of 100 μF and a dc voltage of 240 V. What is the amount of energy stored in the capacitor? (Answer: 2.88 J.) The flash discharges the stored energy in approximately 1/2000 sec making it very bright. What is the power level during the discharge? (Answer: 5.76 kW.)

Capacitances of capacitors used in electronics can vary over a wide range. Small capacitors from pF to nF are mostly ceramic disc capacitors. Capacitors in the μF range are electrolytic capacitors. A capacitor is labeled with either its capacitance or a numerical code. Capacitors with a capacitance above 1 μF or below 100 pF have their capacitances labeled. Capacitors between 100 pF and 1 μF often use the numerical code. Similar to how a resistance is coded in color bands, the code for capacitors includes two significant digits followed by the multiplication factor in unit of pF. For example, code 104 represents 10×10^4 pF, i.e., 0.1 μF. In addition to capacitance, you can also find rated voltage and tolerance on the capacitor. For example, letter "K" represents 10% tolerance. Electrolytic capacitors must be placed in the circuit with the proper polarity. The polarity of a capacitor is indicated by either a white stripe marked with a minus sign for the negative lead or an arrow marked with a positive sign for the positive lead. The negative lead should be connected to a node with a lower dc voltage. If the polarity is incorrect, an electrolytic capacitor can carry a leakage current affecting the bias condition of the circuit. Make sure that the peak voltage across any capacitor is always below its rated maximum voltage. Operating above the limit, an electrolytic capacitor can explode and become a hazard.

Inductors are formed by winding a conducting wire to form a coil in the air or around a ferrite core. They are used in power and radio frequency (RF) electronics. When two coils are closely coupled via a common magnetic core, the mutual inductance creates a transformer. Transformers can vary the ac voltage in the power grid and provide impedance matching in RF circuits. Inductor generates a voltage when it carries a time-varying current according to the Faraday's law:

$$V(t) = L\frac{dI(t)}{dt}. \tag{6}$$

Although we often use voltage and current as variables in circuit analysis, there are also the electric field and the magnetic field. In a capacitor formed by two parallel metallic plates with an area of A and a separation of d, the electric field is:

$$E = \frac{V}{d} = \frac{Q/A}{\varepsilon}, \tag{7}$$

where ε is the dielectric constant of the medium. The ratio, Q/A, is the charge per unit area. From the above equation, can you determine the capacitance using variables A, d and ε?

(Answer: $\varepsilon A/d$.) The Ampere's law determines the magnetic field around an infinitely long conducting wire carrying a current of I.

$$B = \frac{\mu_0 I}{2\pi r}, \tag{8}$$

where μ_0 is the permeability of the free space and r is the radial distance from the center of the wire. At the radio frequency, fields create radiation and coupling among wires and components, hence, crosstalk and electromagnetic interference (EMI).

To learn something entirely new, a textbook is still the most valuable guide. Materials in this chapter are covered in any college physics textbook, such as, "Fundamentals of Physics," by David Halliday, Robert Resnick and Jearl Walker. For people who already have some background knowledge, the Internet is the most resourceful, public "library." To make efficient use of time, users need to search with the right keywords and discern the information. For materials covered in this chapter, readers may find the following website, http://web.mit.edu/sahughes/www/8.022/, useful.

2. Essential Circuit Analysis

In this chapter, we provide a brief review of circuit analysis. Most circuits discussed in this chapter will appear in subsequent chapters.

A circuit is constructed by connecting components together. A node is where two or more components join. Loop represents a complete path for the current to flow. The first circuit consists of two resistors, R_1 and R_2. They are connected in series forming a voltage divider. The circuit diagram is shown below. In the circuit, there is a voltage source which provides a dc voltage to drive the circuit. Battery and dc power adapter are examples of a dc voltage source. The ground node marked with an inverted triangle serves as a reference for zero voltage.

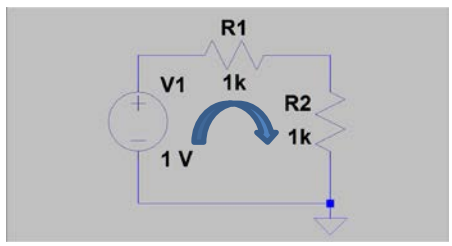


Fig. 1. The diagram of a voltage divider circuit.

There is one loop carrying a current, I. The input voltage is V_1. The output node is located at the upper right-hand corner, where R_1 and R_2 join. The Kirchhoff's voltage law states that the sum of all voltages across components in a complete loop must be zero. Starting from the ground node, we have a power supply which raises the voltage by $+V_1$, a reduction of voltage across R_1 by $-I \cdot R_1$ and another voltage drop by $-I \cdot R_2$. For a current flowing in the clockwise direction, I is positive. Please note that signs are very important in circuit analysis. According to the Kirchhoff's voltage law:

$$+V_1 - IR_1 - IR_2 = 0. \tag{1}$$

After solving for I in the above equation, one can find that the output of the voltage divider is:

$$V_O = IR_2 = V_1 \cdot \frac{R_2}{R_1+R_2}. \tag{2}$$

The input voltage is divided between two resistors according to their resistances. The lower the R_2, the smaller is the output voltage. When both resistances are 1 kΩ, the dividing ratio is 2. What is the dividing factor when R_1 is 1 kΩ and R_2 is 47 Ω? (Answer: 21.)

The second circuit is shown in Fig. 2. It is a Wheatstone bridge circuit used for sensing.

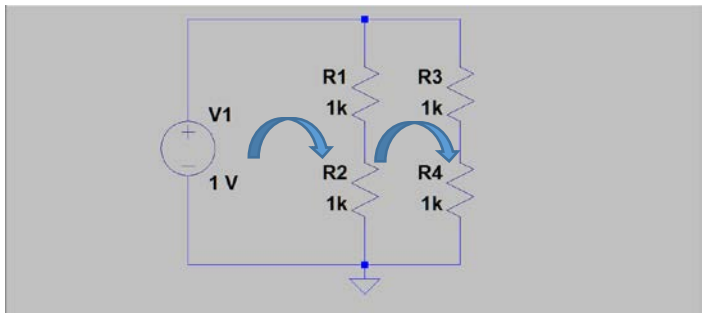


Fig. 2. The circuit diagram of a bridge circuit.

Two resistors, R_1 and R_2, form the left arm. The other two resistors, R_3 and R_4, form the right arm. In sensing applications, one of the resistors is replaced by a sensor, such as a thermistor. The voltage difference between two elbow nodes correlates with the temperature.

The circuit consists of two current loops with I_1 and I_2 flowing in the clockwise direction, respectively. The Kirchhoff's current law states that the sum of the current flowing into a node must be balanced by the current flowing out and away from the node. A current of I_1 flows into the upper node while I_2 flows away from it. Therefore, the current flowing into R_1 must be I_1-I_2. This same current also flows through R_2 because it is in series with R_1. Now we can apply the Kirchhoff's voltage law to set up two equations, one for each loop:

$$V_1 - (I_1 - I_2) \cdot (R_1 + R_2) = 0, \tag{3}$$

$$V_1 - I_2 \cdot (R_3 + R_4) = 0. \tag{4}$$

Variables, V_1, R_1, R_2, R_3 and R_4, are known. From two equations, we can solve for two variables, I_1 and I_2. It is straight forward to find:

$$I_1 = V_1\left(\frac{1}{R_1+R_2} + \frac{1}{R_3+R_4}\right). \tag{5}$$

The analysis of the bridge circuit can be simplified by considering two independent branches or arms, one on the left consisting of R_1 and R_2 in series; the other on the right consisting of R_3 and R_4 in series. Both branches share a common voltage source, V_1. Instead of setting up loop equations, we can simply write down the current of each branch. With V_1 at 1 V and four 1-kΩ resistors, there is a current of 0.5 mA flowing in each branch.

In circuit analysis, when there are multiple loops, hence, a large number of variables, one needs to apply linear algebra and use matrix operations to solve for variables. The fewer the number of variables and the fewer the number of loops, the simpler is the analysis. Techniques, such as Thévenin or Norton transformation, principle of linear

superposition, etc., can reduce the number of loops, hence, variables and simplify circuit analysis.

To characterize circuits with capacitors or inductors, we use ac signals. The sinusoidal signal facilitates characterizations of circuits in the frequency domain. By scanning the frequency of the input sinusoidal signal, characteristics of the circuit as a function of frequency can be measured. The span from the positive peak to negative peak is the peak-to-peak voltage. For a sine wave, the peak-to-peak voltage corresponds to two times the amplitude. The product of period, *T*, and frequency, *f*, is unity. A 1-kHz signal has a period of 1 msec. The percentage delay within each cycle corresponds to a phase shift, between 0 and 2π or 360^0. The square-wave signal provides information on how fast a circuit can respond to an abrupt change at the input. It is used to characterize digital circuits in the time domain.

The next circuit to construct is an RC filter circuit consisting of a resistor and a capacitor. Like the voltage divider circuit, the output node is located at the upper right-hand corner, i.e., across the capacitor. At very low frequencies, a capacitor behaves like an open circuit. The input voltage appears fully at the output. This is a low-pass filter circuit.

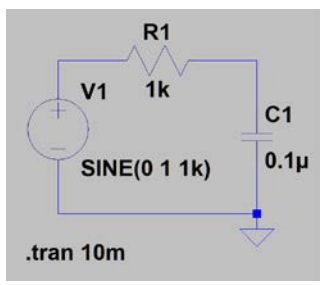


Fig. 3. The diagram of an RC filter circuit. The output is across the capacitor. It is a low-pass filter circuit.

For a sine wave, the complex representation of the voltage is given by:

$$V(t) = V \cdot e^{j\omega t}, \tag{6}$$

where $j = \sqrt{-1}$. The only time dependence is in the exponent. The time differentiation of *V(t)* becomes a multiplication by a factor of $j\omega$. The impedance of a device is defined as the ratio of voltage and current. The impedance of a resistor is real. Its value is simply *R*. The impedance of a capacitor is complex and frequency-dependent:

$$Z_c = \frac{1}{j\omega C}. \tag{7}$$

With impedances, we can analyze the RC circuit like a voltage divider. The ratio between the output, V_o, and input, V_{in}, of the low-pass filter is:

$$\frac{V_o}{V_{in}} = \frac{1/j\omega C}{R+1/j\omega C} = \frac{1}{1+j\omega/\omega_0} = \sqrt{\frac{1}{1+\omega^2/\omega_0^2}} \cdot e^{-jtan^{-1}\frac{\omega}{\omega_0}}, \quad (8)$$

where ω_0=1/(R·C). It is the angular frequency, 2πf_0, at which the amplitude of the output voltage is reduced by a factor of 1/√2 or down to 70.7%. Since the power is proportional to the square of voltage, the power is reduced to 1/2 or 50%. Therefore, f_0 is called the -3 dB frequency of the low-pass filter. Decibel or dB is defined as 10·$\log_{10}$ (P_{out}/P_{in}) or 20·$\log_{10}$ (V_{out}/V_{in}) for the sine wave signal. With 1 kΩ and 0.1 μF, what is the -3 dB frequency? (Answer: 1.59 kHz.) When the frequency is low, the amplitude of the output is nearly unity and the phase angle is zero.

A square wave, clock signal is also used in characterizing the transient response of circuits, especially, digital circuits. The response of the RC circuit to an externally applied signal is governed by the Kirchhoff's voltage law:

$$RC\frac{dV_c}{dt} + V_C = V_S. \quad (9)$$

The voltage across the capacitor is V_C. The voltage of the signal source is V_S. This is a first-order differential equation with constant coefficients. The general form of a first-order differential equation is:

$$\frac{dy}{dt} + Ay = B. \quad (10)$$

It has the following general solution:

$$y(t) = c_1.e^{-At} + c_2. \quad (11)$$

A converging solution exists only when A is positive. The constant, c_1, is determined by the boundary condition at time zero and the value of c_2. The constant, c_2, is determined by the boundary condition at time infinity. A boundary condition represents the physical state of the system at a specific time. For a step input signal with an abrupt rise of voltage from -1 V to 1 V at time zero, the boundary conditions are -1 V before time zero and +1 V at time infinity, the voltage across the capacitor is:

$$V_c(t) = -2e^{-\frac{t}{RC}} + 1. \quad (12)$$

The capacitor accumulates the charge delivered by the current to generate the output voltage. Therefore, a low-pass filter is an integrator. The main application of the low-pass filter is to suppress the high-frequency noise.

By exchanging locations of resistor and capacitor in the circuit, we obtain a high-pass filter. The input signal is connected to capacitor and the output is across the resistor. The high-pass filter attenuates the signal at low frequency and passes through the signal at high frequency. For the transient response, the output signal peaks when the input signal makes a sharp transition. It is a differentiator.

Similarly, one can analyze RL circuits. For the frequency domain analysis, one can use the complex impedance of the inductor:

$$Z_L = j\omega L. \tag{13}$$

What is the -3 dB frequency of an RL filter? (Answer: $R/(2\pi L)$.) For the transient response, one can solve the following first-order differential equation:

$$L\frac{dI}{dt} + RI = V_s. \tag{14}$$

As boundary conditions, the current of the inductor is $-V_s/R$ just before and $+V_s/R$ long after a positive step input is applied. The symbol, V_s, is the amplitude of the square-wave signal.

After analyzing RC and RL circuits, we can proceed to analyze the RLC circuit. There are two configurations, one with LC in series and the other in parallel. Shown below is a circuit with LC in series.

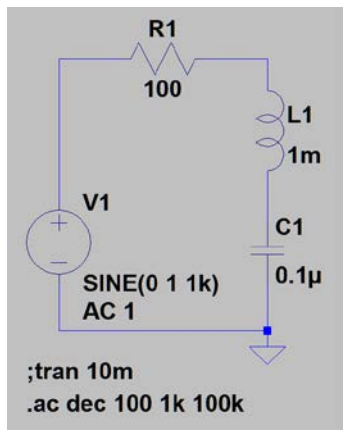


Fig. 4. The diagram of the series RLC circuit.

Using the total complex impedance of LC in series, we can calculate the output voltage across LC.

$$V_{out} = \frac{j\omega L + \frac{1}{j\omega C}}{R + j\omega L + \frac{1}{j\omega C}} \cdot V_{in} = \frac{1-\omega^2 LC}{(1-\omega^2 LC) + j\omega RC} \cdot V_{in}. \tag{15}$$

There is a resonance frequency at:

$$f_0 = \frac{1}{2\pi\sqrt{LC}}. \tag{16}$$

At the resonance frequency, the output is zero. This is true in theory. However, for an inductor with a finite resistance, the output is low but not exactly at zero.

To study the transient response of the RLC circuit, we can apply the Kirchhoff's voltage law and boundary conditions.

$$IR + L\frac{dI}{dt} + \frac{1}{C}\int I dt = V_s. \tag{17}$$

Differentiate the above equation with respect to time leads to the following second-order differential equation.

$$L\frac{d^2I}{dt^2} + R\frac{dI}{dt} + \frac{I}{C} = \frac{dV_S}{dt}. \tag{18}$$

With a step voltage as input, the right-hand side of the equation is zero except at time zero. The general form of the second-order differential equation with constant coefficients is

$$a\frac{d^2y}{dt^2} + b\frac{dy}{dt} + cy = 0. \tag{19}$$

The type of solution depends on whether b^2-$4ac$ is positive or negative. When it is negative, the general solution is

$$y(t) = e^{-\alpha t}(c_1\cos(\beta t) + c_2\sin(\beta t)), \tag{20}$$

where $\alpha=b/2a$ and $\beta=\sqrt{(b^2-4ac)}/2a$. The solution has the form of a damped relaxation oscillation. Boundary conditions of y and its time differentiation at time zero determine values of two constants, c_1 and c_2.

$$c_1 = y(0), \tag{21}$$

$$c_2 = \frac{y'(0)+\alpha c_1}{\beta}. \tag{22}$$

Let's consider the boundary conditions for the current. Responding to a sudden change in voltage, the inductor generates an opposing voltage to prevent the current from rising instantaneously. Long after the transient switching, the capacitor blocks the current from flowing. Therefore, $I(0)=I(\infty)=0$. Current only flows during the transient stage in the form of a damped relaxation oscillation. The boundary condition of $I'(0)$ can be determined from Eq. (17). It is $[V_S(0+)-V_S(0-)]/L$. With coefficients in the differential equation and boundary conditions known, can you write down the closed form solution explicitly?

Similarly, we can construct an RLC circuit with an inductor and a capacitor in parallel.

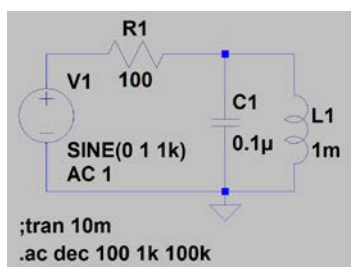


Fig. 5. The diagram of an RLC circuit with L and C in parallel.

When two components are in parallel, we add the inverse impedance, $1/Z$, or admittance, Y, to obtain the overall admittance.

$$\frac{1}{Z} = \frac{1}{Z_1} + \frac{1}{Z_2}. \tag{23}$$

The frequency domain response is determined by:

$$V_{out} = \frac{\frac{1}{j\omega C+\frac{1}{j\omega L}}}{R+\frac{1}{j\omega C+\frac{1}{j\omega L}}} \cdot V_{in} = \frac{j\omega L}{R\cdot(1-\omega^2 LC)+j\omega L} \cdot V_{in}. \tag{24}$$

At the resonance frequency, the real part of the denominator is zero. The throughput is unity. The phase angle is zero. Away from the resonance frequency, the throughput gradually diminishes. To analyze the circuit in the time domain, one needs to set up and solve a differential equation with boundary conditions.

Similar to textbooks, there are equations in this chapter. Readers can appreciate why calculus, differential equations and linear algebra are essential for electrical engineers. After knowing how to analyze circuits, one can rely on simulations to obtain the characteristics of circuits. The interpretation of simulation results, however, requires a solid understanding of circuit analysis. In the next chapter, you will find results of simulations for all circuits discussed in this chapter.

For materials covered in this chapter, readers may find the following website, www.khanacademy.org/science/electrical-engineering/ee-circuit-analysis-topic, useful.

3. Circuit Simulations - LTspice

To learn electronics using the empirical approach, we need a tool to enable users to easily modify circuits and observe outcomes. Based on correlations between the input and output, readers can deduce the characteristics of circuits and learn how to optimize them. In this chapter, we will discuss a circuit simulation program, LTspice, and use it to study characteristics of R, C and L circuits discussed in Chap. 2.

LTspice is made available by Linear Technology, now part of Analog Devices. Download and install LTspice from: http://www.analog.com/en/design-center/design-tools-and-calculators/LTspice-simulator.html. The components in the build-in library are mostly products of Linear Technology and Analog Devices. Users can add additional devices to the library. There are tutorials available online. This chapter starts with an introduction for the Windows version of LTspice to get you started. You can search online to find a tutorial for the Mac version.

After you launch LTspice, click "File", then "New Schematic". Click "Edit" to place resistor, capacitor, inductor, diode and other components in the schematics and compose a circuit diagram. Under "Component", you can find "voltage" source and semiconductor devices, such as "npn" and "pnp" bipolar junction transistors, "njf" and "pjf" junction field-effect transistors, "nmos" and "pmos" metal-oxide-semiconductor field-effect transistors, etc. By clicking "Opamps", you can find operational amplifier models available in the library as sub-circuits. After placing a component, you can stop repeating the same component by right clicking or by pressing the Esc key. You can click "Edit", "Move", then select the component or a group of components within an area to move. If you want to change the orientation of a component, you need to click "Edit", "Rotate" after selecting the component. You can right click a component to change its value or model number. Click "Edit", "Place GND" to place the ground node. The ground node is the reference for zero voltage. Click "Edit", "Draw Wire" to connect components. Save the schematics after composing the circuit diagram.

The first circuit to build is a voltage divider. The circuit diagram with both resistors at 1 kΩ is shown below. The input voltage is V_1. The output node is located at the upper right-hand corner, i.e., junction of R_1 and R_2.

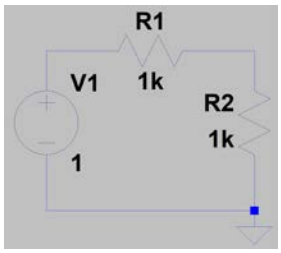
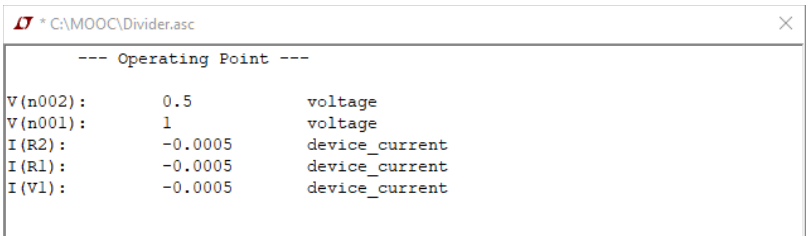


Fig. 1. The diagram of a voltage divider circuit.

Since the signal source is dc, we can simulate the dc voltage and current. Click “Simulate” and click “dc op pnt” for dc operating point. Click OK and place the SPICE Directive “.op” in the schematics. Click “Simulate”, then “Run”. The result appears in the “Operating Point” window as shown below.



```
* C:\MOOC\Divider.asc

       --- Operating Point ---

V(n002):        0.5             voltage
V(n001):        1               voltage
I(R2):          -0.0005         device_current
I(R1):          -0.0005         device_current
I(V1):          -0.0005         device_current
```

Fig. 2. Results of the dc operating point simulation of the voltage divider circuit.

The voltage at node 2, which is the output node of the voltage divider, is 0.5 V. The source voltage is divided between two resistors. You can always identify the node number by moving the cursor to the node in the schematic diagram. The node number is displayed at the lower left corner. As shown in Fig. 2, there is a current of -0.0005 A or -0.5 mA. The sign is positive when the current flows in the counterclockwise direction. The sign is negative when the current flows in the clockwise direction.

The next circuit to draw and simulate is an RC filter circuit consisting of a 1-kΩ resistor and a 0.1-μF capacitor placed in series. Just like the voltage divider circuit, the output node is located at the upper right-hand corner. This is a low-pass filter circuit.

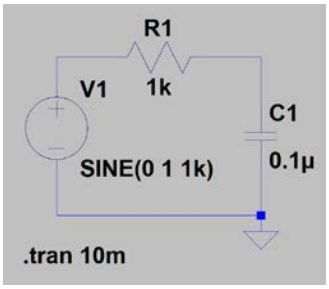


Fig. 3. The diagram of the RC filter circuit. The output is across the capacitor. It is a low-pass filter circuit.

To define the signal source, right click on it. Choose “Advanced”. Highlight the sine wave. Enter 0 or leave it blank for the dc offset. Set the amplitude to 1 (V) and the frequency to 1k (Hz). Click “Simulate” and “Edit Simulation Cmd”. Choose “Transient” for time-domain simulations. Enter the stop time as 10m. Since the frequency of the signal is at 1 kHz, there are 10 cycles in 10 msec. Place the SPICE directive for transient simulation in the schematics. Run the simulation. After the simulation is completed, there is a display pane showing up. Click the top node of V_1 to see the input waveform. Click the output node at the top of capacitor to see the output waveform. You can also right click and add a trace by entering the node name, e.g., V(n001). Furthermore, you can add a trace using a mathematical formula, e.g., (V(n001)-V(n002))/1. Such a formula facilitates the plot of current in mA of a 1-kΩ resistor. You can also display the current by pointing the mouse around the node of a component. A red arrow appears indicating the direction of current along with a loop indicating a current probe. Click the mouse to display the current. You can change the color by right clicking the label on the top of the display. The result is shown below. The graph is presented as is so that you know what to look for when you simulate the circuit.

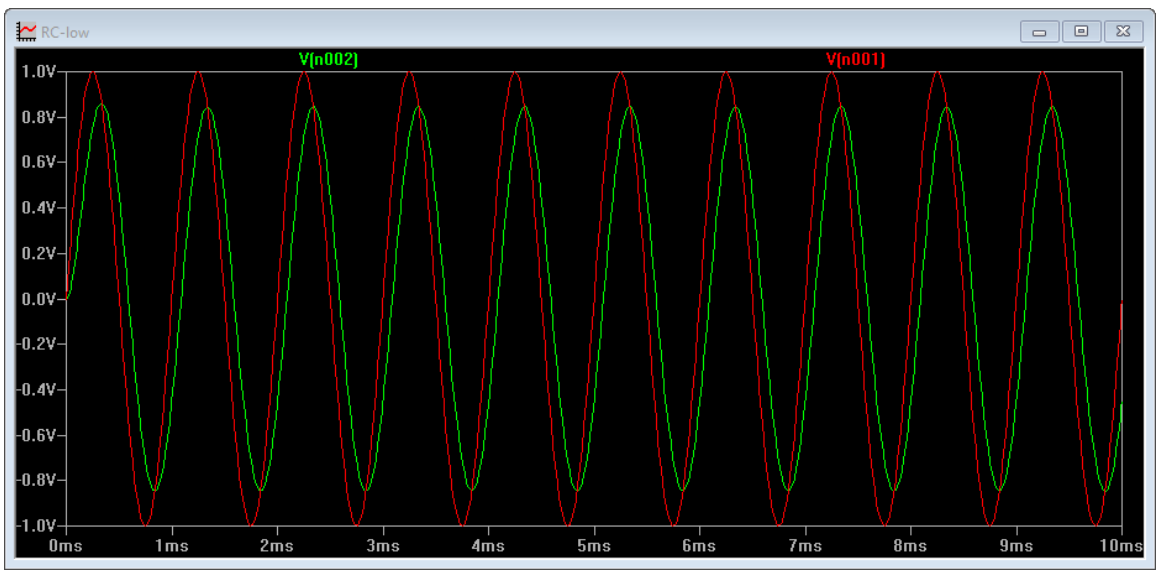


Fig. 4. The input signal shown in red and the output waveform shown in green color of the low-pass filter.

The waveform data can be exported to a text file. Click and highlight the top frame of the waveform display pane. Click “File” then “Export data as text” to save the data. In the

file, the first column is the time. The second and subsequent columns store the voltage or current data.

To see the response of the circuit as a function of frequency, edit the simulation command. Choose “ac Analysis”. Set the type of sweep to “Decade”, number of points to 100, start frequency to 10 and stop frequency to 100k. Of course, the unit of frequency is Hz. Place the SPICE directive in schematics. Right click the signal source, V_1. In “Small signal ac analysis” enter 1 for “ac Amplitude.” You should use an amplitude that will not cause waveform clipping in the time domain. Click OK. Run the simulation. Click the output node to add the trace. Here is what you will observe.

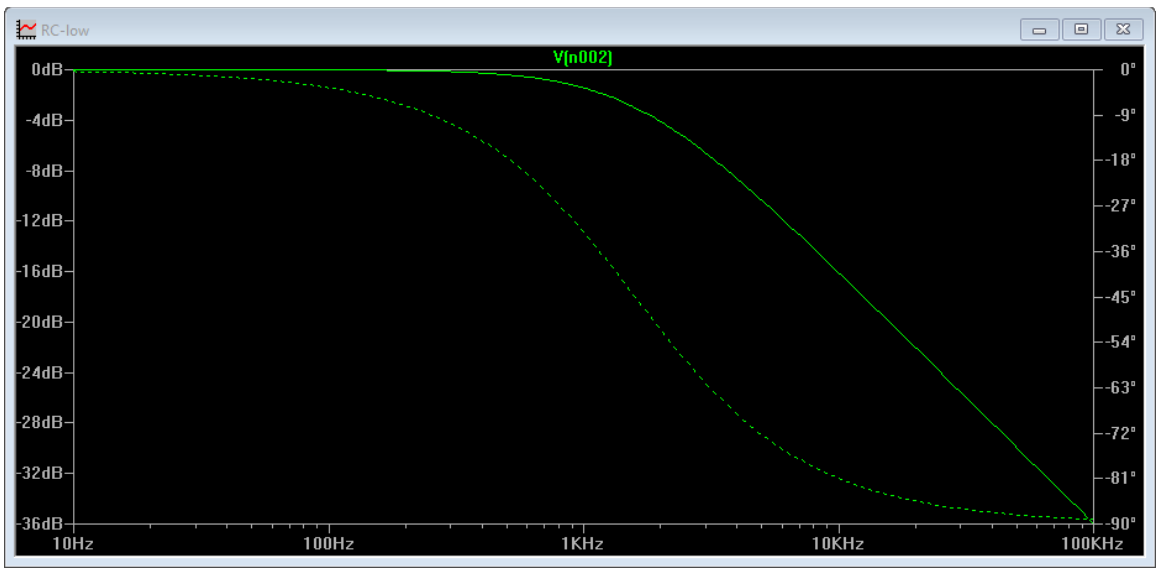


Fig. 5. The Bode plot showing the throughput and phase of the low-pass filter as a function of frequency.

The amplitude is represented by the solid curve with its scale on the left side. The phase is shown as the dotted curve with a scale on the right side. The horizontal frequency axis is in the $\log_{10}$ scale to cover multiple orders of magnitude. The vertical axis on the left side is in dB unit. The solid curve presents 20 $\log_{10}$(Vout/Vin). The vertical axis on the right side shows the phase angle of the output signal in degree. The amplitude decreases and the phase angle approaches asymptotically to -90^0 as the frequency increases. Low frequency signal passes through without attenuation while high-frequency signal is attenuated.

You can observe the transient response of the low-pass filter to a square-wave input in the time domain. Change V_1 to “Pulse”. Set “Vinitial” to -1, Von to 1, Trise to 10n, Tfall

also to 10n, Ton to 500u and Tperiod to 1m. The rise and fall time of the 1-kHz square wave is arbitrarily set to 10 nsec. Edit the simulation command for transient simulation. Run the simulation. Click the input node and output node to display the waveforms. You can zoom in to see the rising or the trailing transition. Click and press the left button of the mouse to select the left upper corner of the region to zoom in. Drag the mouse to the lower right corner of the region to zoom in. Release the button. To zoom out, right click and select Zoom to Fit.

To save the waveforms as data, click the top light blue frame of the waveform display pane. Click “File,” “Export data as text.” You can open the file with Excel using the default setting. There are three columns corresponding to time, waveform #1 and waveform #2.

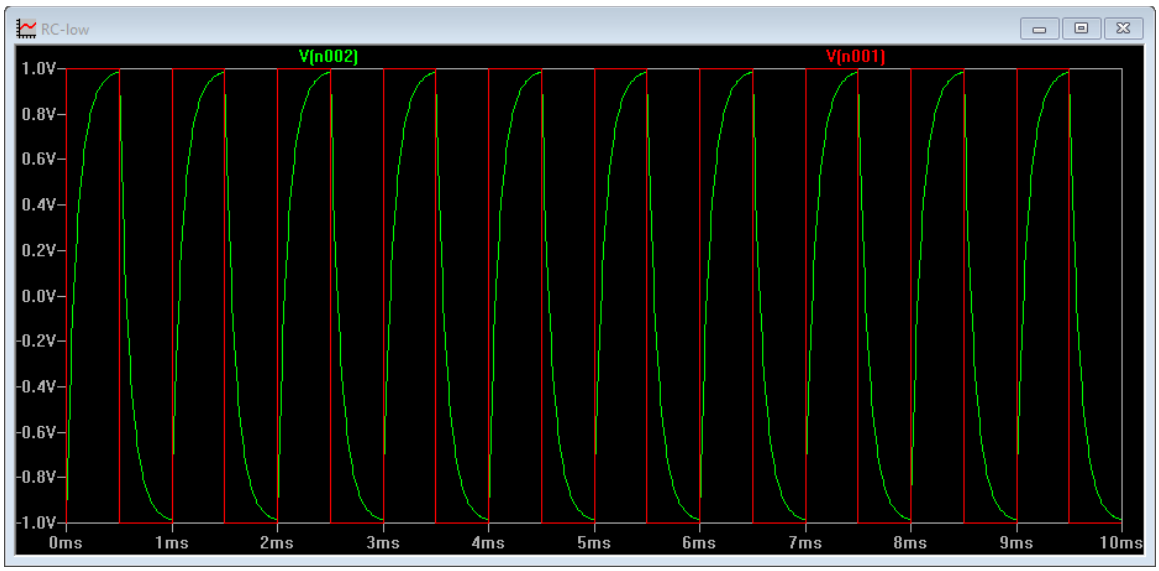


Fig. 6. The input square wave shown in red and the output waveform shown in green color of the low-pass filter.

By exchanging positions of resistor and capacitor in the circuit, we obtain a high-pass filter. The input signal is connected to capacitor and the output is across the resistor. Under the same driving conditions, waveforms of the high-pass filter are shown below for sine wave and square-wave excitations, respectively.

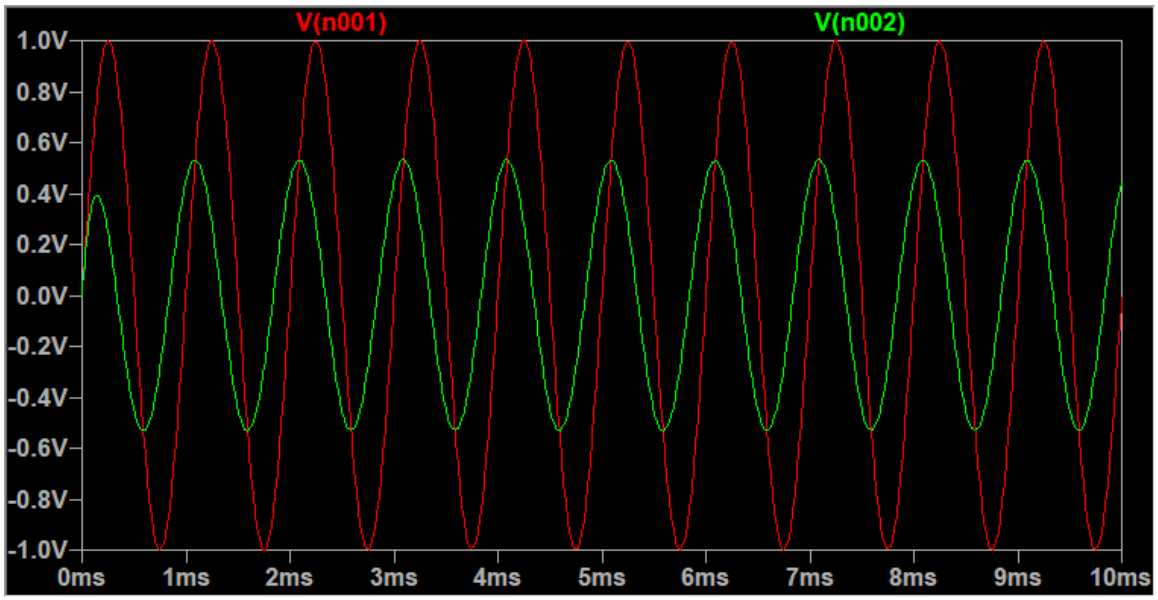


Fig. 9. The input and output waveforms of the high-pass filter. The input is shown in red and output in green color.

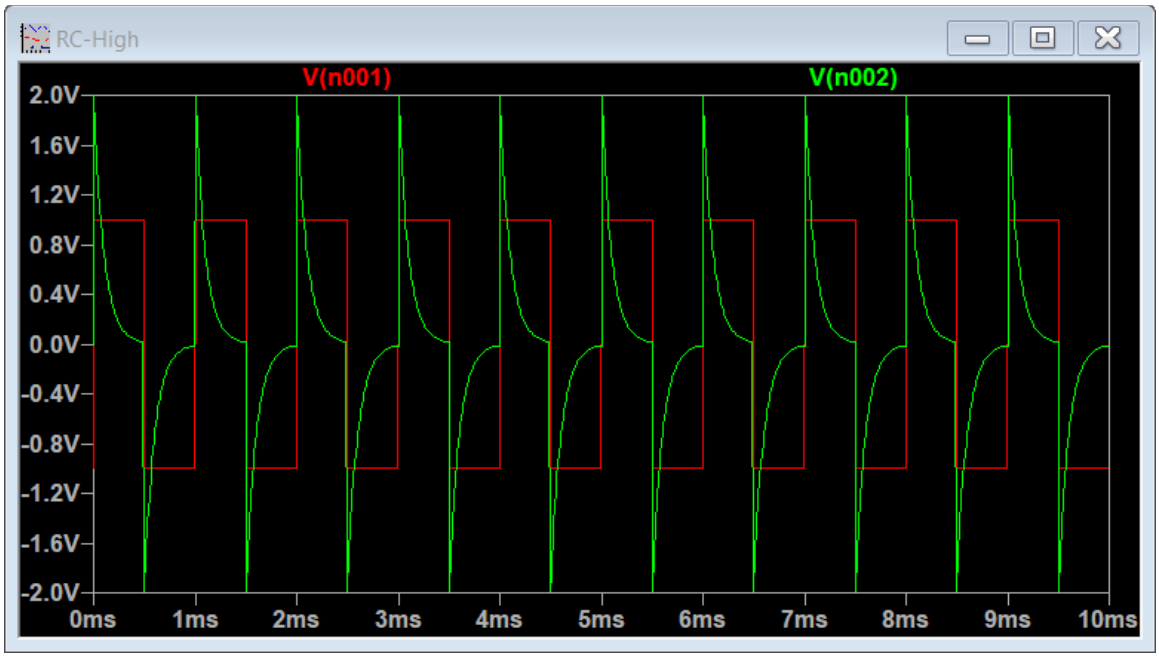


Fig. 10. The response of a high-pass filter. The red trace is the input square wave. The waveform shown in green color is the output voltage across the resistor.

With sinusoidal signal input, the frequency response is shown in the following Bode plot:

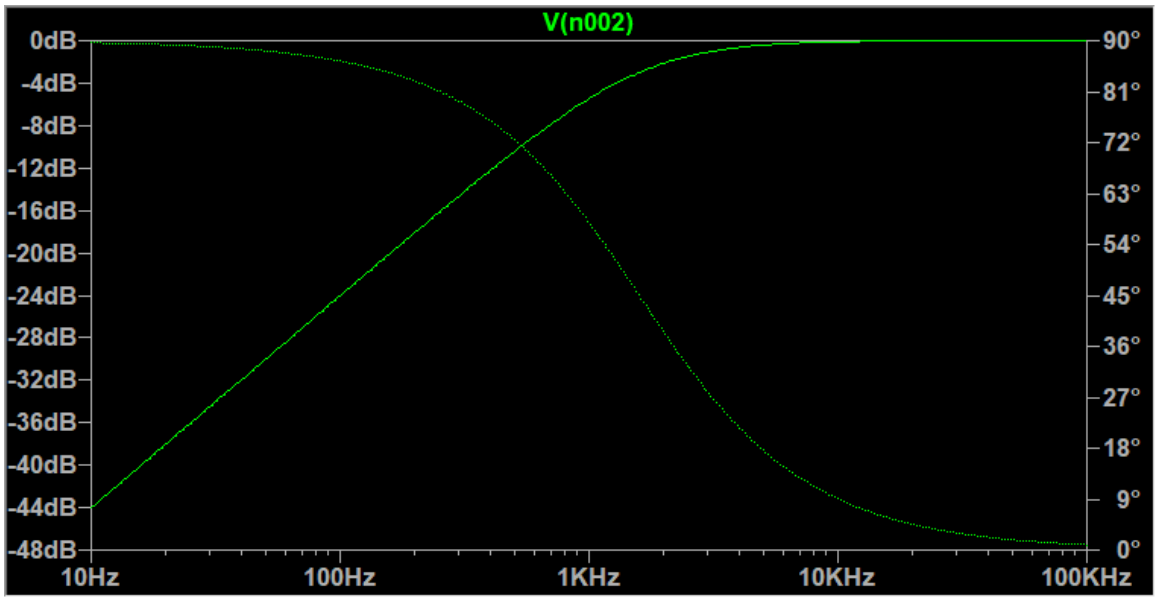


Fig. 11. The Bode plot showing the throughput and phase of the high-pass filter as a function of frequency.

Similarly, one can draw and simulate RL circuits. The next circuit to simulate is the RLC circuit. There are two configurations, one with LC in series and the other in parallel. Shown below is the circuit with LC in series.

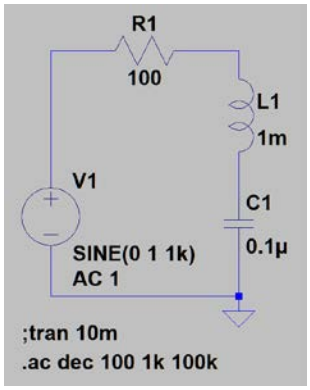


Fig. 12. The diagram of the series RLC circuit.

You can right click the inductor. Enter a series resistance of 10 (Ω). Shown below is the Bode plot obtained by performing the ac analysis. The resonance frequency is at 15.9 kHz. The output is approximately -21 dB or two orders of magnitude below the input.

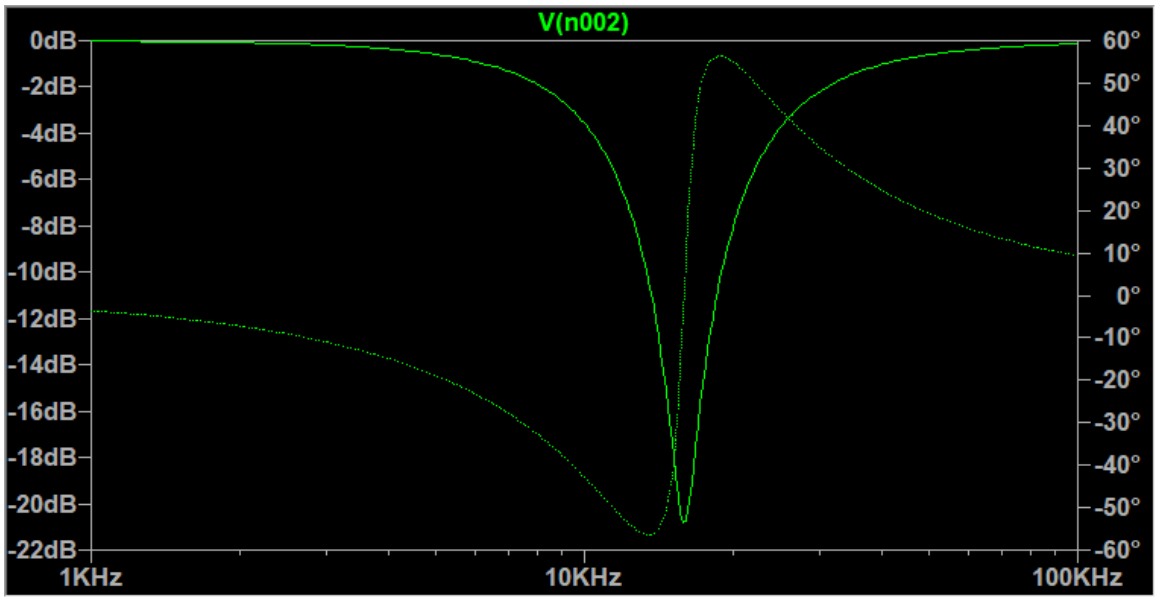


Fig. 13. The Bode plot showing the power throughput and phase of the series RLC circuit as a function of frequency.

Shown below is the result of the transient simulation. The input square wave is presented in red. The current in the resistor is presented in green color.

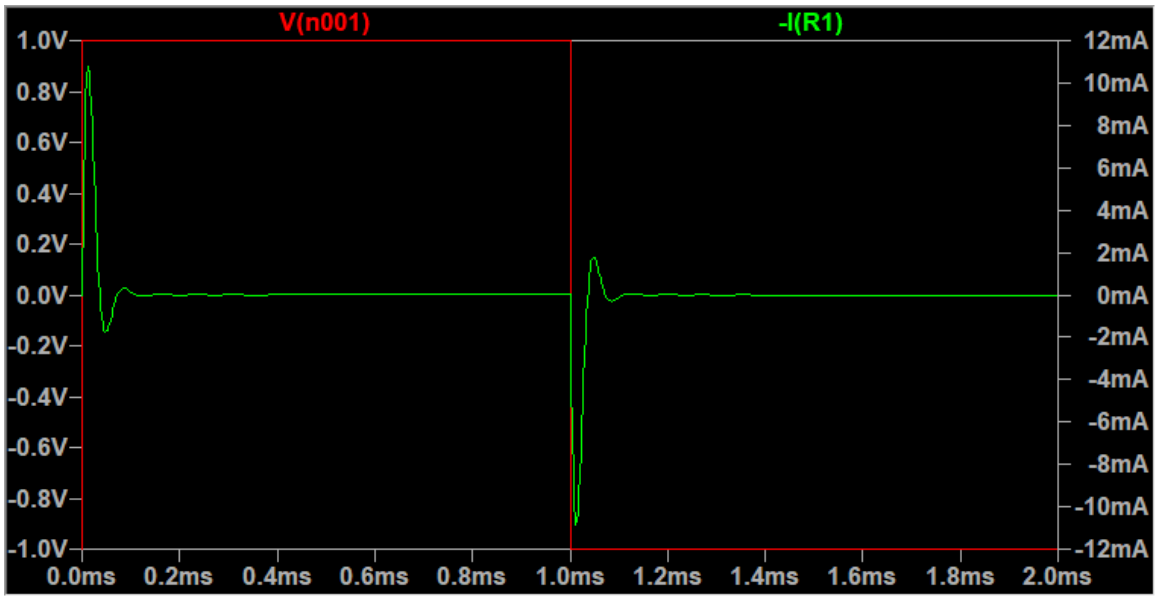


Fig. 14. The response of a series RLC circuit. The red trace is the input step voltage. The waveform shown in green color is the current going through L and C in series in the clockwise direction.

Similarly, we can compose and simulate an RLC circuit with inductor and capacitor in parallel.

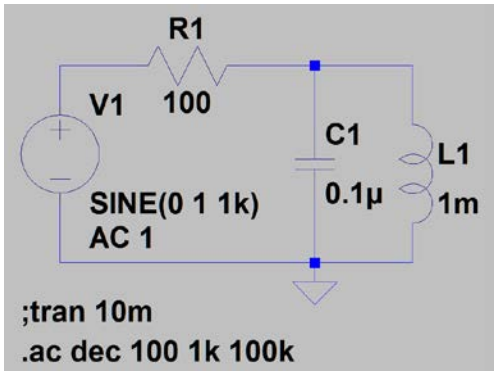


Fig. 15. The diagram of the RLC circuit with L and C in parallel.

Shown below in the simulated Bode plot.

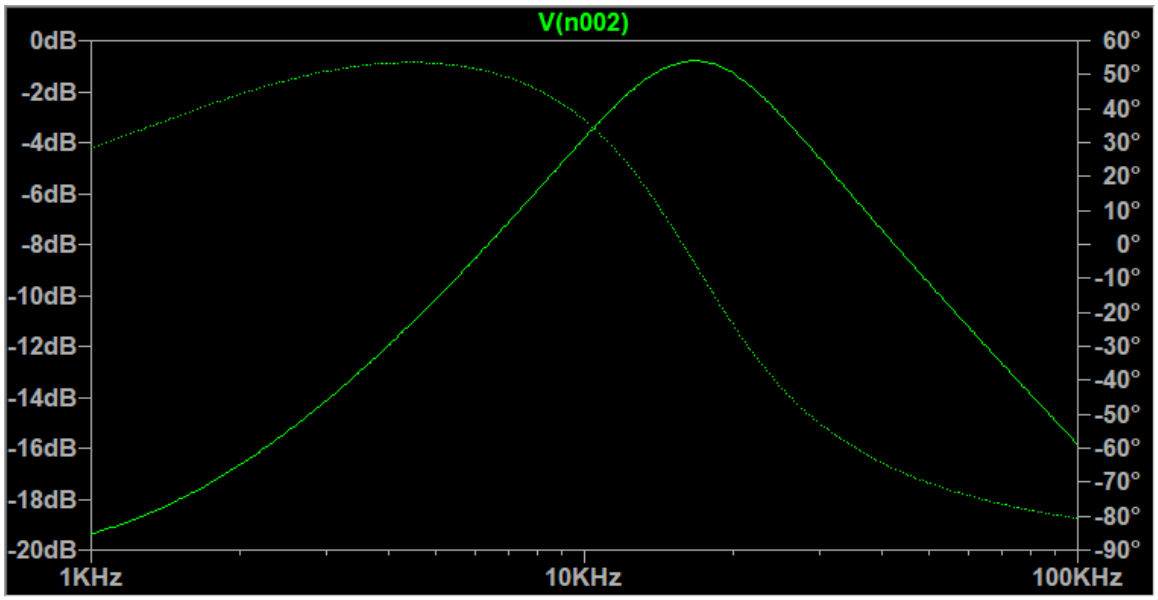


Fig. 16. The Bode plot showing the power throughput and phase of the RLC circuit with L and C in parallel as a function of frequency.

You can drive the circuit with a square wave and determine the current. The current has a transient spike followed by a damped relaxation oscillation before reaching the steady state as shown in Fig. 17.

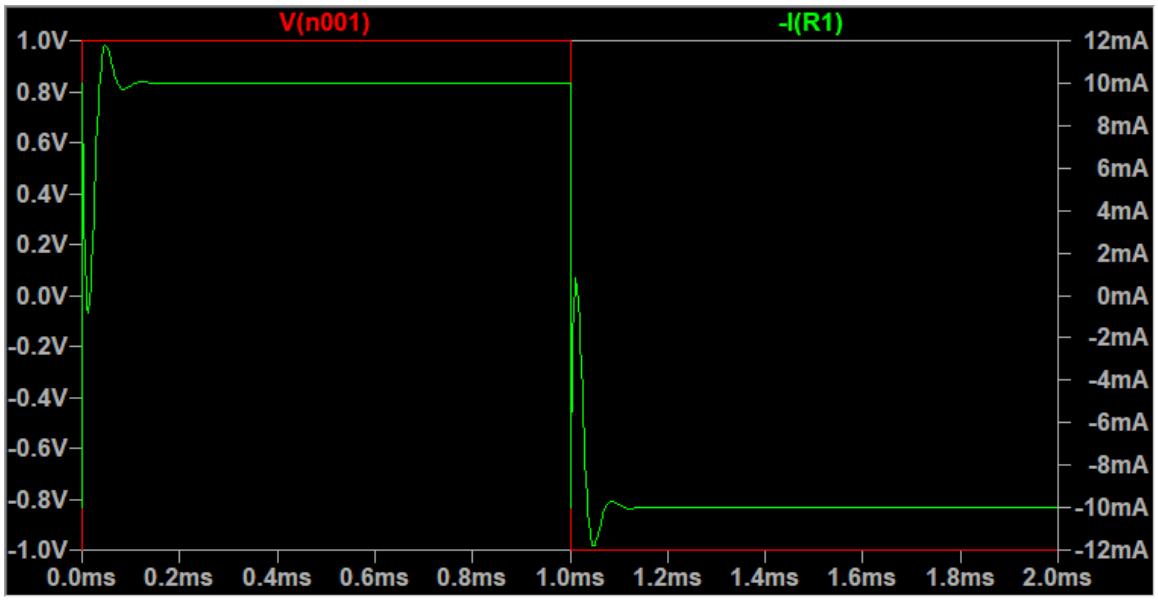


Fig. 17. The response of the RLC circuit with L and C in parallel. The red trace is the input square wave. The waveform shown in green color is the current flowing through R.

There are devices not in the distributed library of LTspice. A zip file is provided to make additional devices available for simulations. Added devices are categorized into two groups. In one group, the symbols and sub-circuits of devices are added as additional sub-directories. Examples include the 74HC series of digital integrated circuits (IC) and analog ICs, such as the 741 operational amplifier. In the second group, the SPICE model of each device is appended to the corresponding device files. Examples include bipolar junction transistor in the CA3046 transistor array, power rectifying diode, Zener diode, diode laser, photodetector and MOS transistors. Download the zip file. Open instruction.doc. Follow the instruction to customize LTspice.

For readers who look for the full functionality with technical details of LTspice, the following website can be useful, http://ltwiki.org. Alternatively, you can search for "scad3.pdf" and read the document.

For those who would like to use a personal instrument module to characterize circuits discussed in this chapter, please read and follow Appendix C.

4. Introduction to Semiconductor Devices

The foundation of electronics is semiconductor physics. Electrons in a semiconductor form energy bands. The conduction band is at a higher energy while the valance band is at a lower energy. There is a moderate energy gap between them. In the conduction band, electrons can move freely from one site to another. In the valance, holes or vacancies of electrons, can also move. Most electronic devices are made of silicon, a group III element. Optoelectronic devices are made of compound semiconductors consisting of group II and group IV elements.

Electrons can be placed into the conduction band by doping with an n-type impurity. Holes can be placed into the valance band by doping with a p-type impurity. A diode is formed by a p-n junction. The flow of current in a diode is controlled by the physics of the p-n junction. On the n-side, there are donors which provide electrons as carriers in the conduction band. On the p-side, there are acceptors which provide holes in the valance band. Electrons diffuse from the n-side to the p-side, likewise, holes from p-side to n-side. As a result, a depletion layer is formed at the junction. The region is positively charged on the n-side and negatively charged on the p-side. The space charge creates an electric field. Carriers drift in the electric field, opposite to diffusion, creating a balance when there is no externally applied voltage. With an external voltage, the current versus voltage (I-V) characteristics of the junction can be described by:

$$I = I_s(e^{V/\eta V_T} - 1), \tag{1}$$

where I_s is the reverse saturation current, η is the ideality factor of the device, and V_T = kT/e. It carries the unit of voltage and is related to the Boltzmann constant, absolute temperature and the elementary charge. At the room temperature, the value is 0.026 V. The current I_s is below 1 μA and η is around 2. The I-V relation is exponential. When a diode is biased positively above the turn-on voltage, it conducts with a very small resistance. In the case of a Si diode, the turn-on voltage is approximately 0.6 V. With a negative bias, a diode carries a very small current, I_s. It behaves like an insulator with a very large resistance.

Under a high reverse bias, a diode eventually operates in the avalanche breakdown regime. When carriers drift in a large electric field, their kinetic energy may become large enough to generate new electron-hole pairs. As the number of carriers multiplies rapidly, an avalanche breakdown takes place. At the breakdown voltage, the current can abruptly

increase. The breakdown voltage is determined by the doping profile of the junction. It ranges from a few volts to few hundred volts. Diodes designed to operate in the avalanche breakdown region are called Zener diodes. They operate under a reverse bias and can serve as voltage references.

Light emitting diodes (LED) and diode lasers are made of compound semiconductors, such as GaAs, InP and GaN. They are also p-n junction devices. Visible LEDs producing red, yellow, green and blue colors are used as indicators and display matrices. Using phosphors, LEDs for illumination can produce white light with a high efficiently. There are also infrared LEDs for remote control and ultraviolet LEDs for detection. An LED operates in a circuit just like a forwardly biased p-n junction diode. By choosing the resistor in series, one can control the current, hence, the brightness of the LED. Typical current of a small LED is 5-50 mA. The turn-on voltage, however, is color dependent. It could range from 1.5 to 4 V. The polarity of the LED is determined by comparing the lengths of two leads. The long lead is the anode and the short lead is the cathode.

Transistors are the basic building blocks of electronic amplifiers. There are two types, bipolar junction transistor (BJT) and unipolar field-effect transistor (FET). In a BJT, there are three regions consisting of n-type, p-type and n-type (npn) or p-type, n-type and p-type (pnp). Both electrons and holes conduct the current. BJTs are current-controlled devices. By applying an input current from base to emitter, the current flowing from collector to emitter can be controlled. In npn BJTs, for example, electrons flow from the emitter through base to the collector. Most electrons reach the collector. Only a small fraction, e.g., 0.5%, recombines with holes while passing through the base region. Holes in the base region are provided by the input base current. A 20-μA base current can, therefore, control the flow of a large, e.g., 4 mA, emitter current. This is the basic operational principle of all BJT amplifiers. Since there is a current flowing through the base, the input impedance of BJTs is low, e.g., <1 kΩ.

An FET has three terminals, namely, source, gate and drain. Only one type of carriers conducts the current in the channel between the drain and source. Electrons conduct in an n-channel FET and holes conduct in a p-channel FET. The gate voltage creates an electrical field either through a reversely biased p-n junction or a metal-oxide-semiconductor (MOS) structure. It modulates the channel, hence, controls the current between the source and the drain. The FETs can operate in either the depletion mode or the enhanced mode. In the depletion mode, the applied gate-to-source voltage reduces the conduction channel. The higher the applied gate voltage, the smaller is the drain current. In the enhanced mode, the

applied gate-to-source voltage creates or enhances the conduction channel. The higher the gate voltage, the larger is the drain current. The ratio between the change of output current and the change in input voltage is the transconductance. The larger the transconductance, the higher is the gain. In FETs designed for small signal amplification, a change of gate voltage by 1 V can swing the drain current by approximately 4 mA. There are also FETs designed for digital switching. They may have a low transconductance but a high switching speed. Since there is no current flowing through the gate, the input impedance of FETs is very high, e.g., >10 MΩ.

Integrated circuits (IC) are formed by having a large number of transistors fabricated on a semiconductor chip. Examples include operational amplifiers, logic ICs, field-programmable gate arrays, digital signal processors, microcontrollers, microprocessors, etc. Modern-day analog, digital and mixed-signal ICs are manufactured by using very sophisticated design software and micro-fabrication facility. The state-of-the-art system on a chip (SOC) ICs consist of more than ten billion transistors. At such a high transistor count, the power dissipation of each transistor must be extremely low. This can only be accomplished by using the complementary metal-oxide-semiconductor (CMOS) circuits. Digital circuits based on CMOS only consume power during the transient switching. By making each device very small, the power budget of SOCs is approximately 1 W per billion transistors.

There are textbooks for readers who would like to learn semiconductor physics and devices systematically. Examples include “Semiconductor Physics And Devices,” by Donald Neamen; “Microelectronic Circuits,” by Adel S. Sedra, Kenneth C. Smith, Tony Chan Carusone and Vincent Gaudet.

In summary, diode, BJT and FET are the fundamental building blocks of electronic circuits. In the integrated form, we have operational amplifiers for analog applications and highly integrated CMOS chips for digital applications.

5. Rectifying Diode and dc Power Supply

A p-n junction diode is formed with donors on one side and acceptors on the other side of the junction. Current flows from the anode p-side to the cathode n-side. It can be controlled by the applied voltage. The picture and symbol of a diode is shown in Fig. 1. The current flows in the direction of the arrow. The silver ring or the vertical bar marks the cathode.

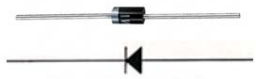


Fig. 1. The picture and symbol of a power rectifying diode.

Draw the circuit shown in Fig. 2.

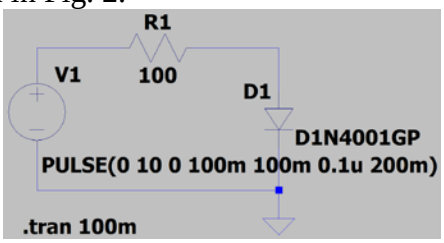


Fig. 2. The circuit to learn the *I-V* characteristics of a diode. The resistance of R_1 can be as low as 100 Ω.

Manual characterization is performed by varying the voltage of the power supply. Record the diode voltage and the diode current. Instead of manual measurements, we can rely on a triangular waveform generator as shown in Fig. 2. Waveforms of the diode voltage and current plotted as a function of time are shown below.

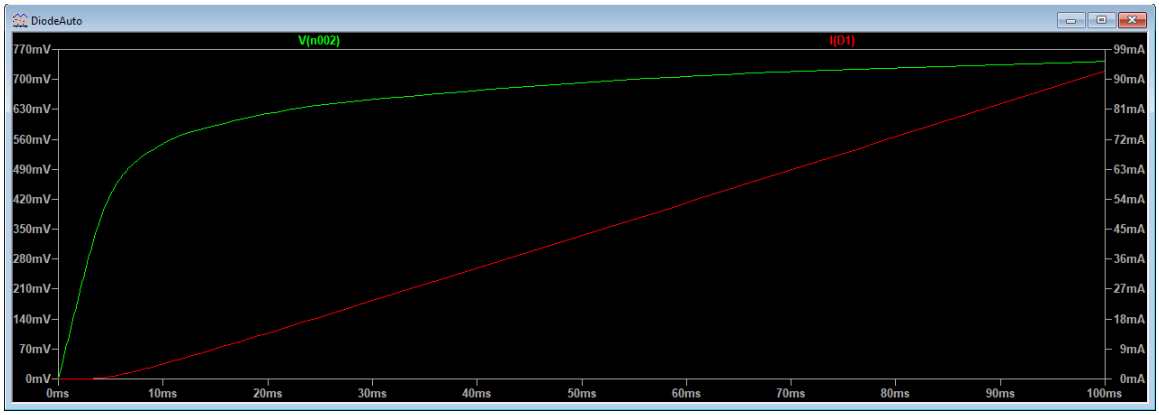
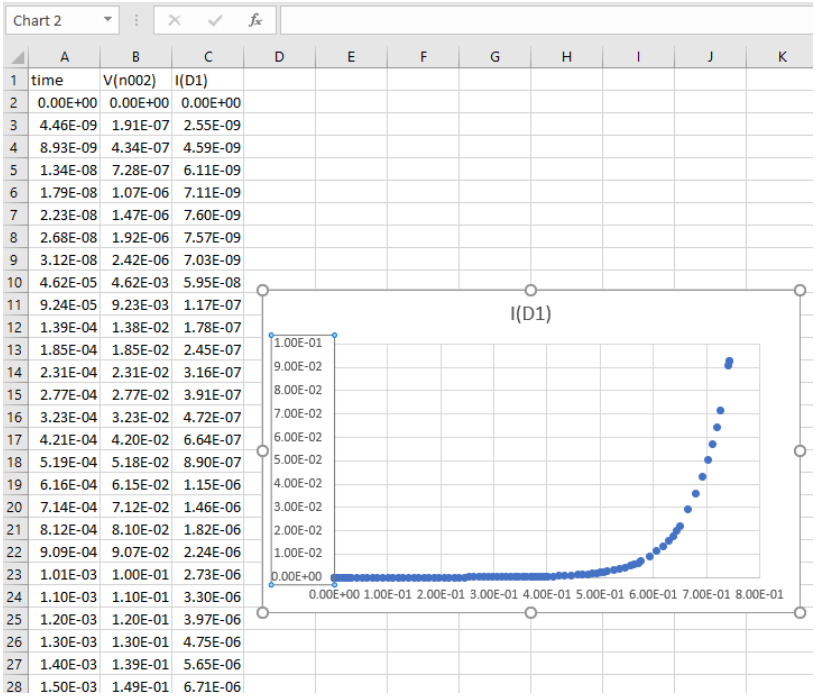


Fig. 3. Waveforms of diode voltage shown in green and current shown in red.

Export the data to a text file. Use Excel to open the text file. Click “Finish” to import the data. Select and highlight columns B and C. Insert a scatter plot to see the I-V characteristics.



	A	B	C
1	time	V(n002)	I(D1)
2	0.00E+00	0.00E+00	0.00E+00
3	4.46E-09	1.91E-07	2.55E-09
4	8.93E-09	4.34E-07	4.59E-09
5	1.34E-08	7.28E-07	6.11E-09
6	1.79E-08	1.07E-06	7.11E-09
7	2.23E-08	1.47E-06	7.60E-09
8	2.68E-08	1.92E-06	7.57E-09
9	3.12E-08	2.42E-06	7.03E-09
10	4.62E-05	4.62E-03	5.95E-08
11	9.24E-05	9.23E-03	1.17E-07
12	1.39E-04	1.38E-02	1.78E-07
13	1.85E-04	1.85E-02	2.45E-07
14	2.31E-04	2.31E-02	3.16E-07
15	2.77E-04	2.77E-02	3.91E-07
16	3.23E-04	3.23E-02	4.72E-07
17	4.21E-04	4.20E-02	6.64E-07
18	5.19E-04	5.18E-02	8.90E-07
19	6.16E-04	6.15E-02	1.15E-06
20	7.14E-04	7.12E-02	1.46E-06
21	8.12E-04	8.10E-02	1.82E-06
22	9.09E-04	9.07E-02	2.24E-06
23	1.01E-03	1.00E-01	2.73E-06
24	1.10E-03	1.10E-01	3.30E-06
25	1.20E-03	1.20E-01	3.97E-06
26	1.30E-03	1.30E-01	4.75E-06
27	1.40E-03	1.39E-01	5.65E-06
28	1.50E-03	1.49E-01	6.71E-06

Fig. 4. Data and the current versus voltage plot of a diode.

From the plot, readers can find characteristics of the Si p-n junction diode. At what voltage does the diode start to conduct? (Answer: around 0.5 V.) What is the voltage when the current reaches 10 mA? (Answer: 0.6 V.) Which function describes the rise of current? (Answer: exponential.) The plot only shows the I-V characteristics with a forward bias. If you extend the triangular wave to the negative voltage, you will find that the reverse saturation current is nearly zero.

The I-V plot offers an opportunity to practice how to deduce device parameters in Eq. (1) of Chap. 3 from the measured data. The second term on the right-hand side of Eq. (1) is much smaller than the first term when the diode conducts. It can be neglected. Readers can apply the $\log_{10}$ function to the equation. What do you get? (Answer: $\log_{10}(I)=\log_{10}(I_s)+0.434V/(\eta V_T)$.) In Excel, format the vertical axis to the logarithmic scale. The I-V plot becomes a line when the current is above 0.1 mA. Extrapolate the line. The intersection of the line with the y-axis is I_s. What is I_s? (Answer: 7×10^{-4} mA.) The slope of the line leads to η. What is η? (Answer: 2.4.)

There is a charge buildup at the junction. The transient response of a p-n junction diode is determined by the charging and discharging of the junction capacitance. Under a reverse bias, the junction capacitance is determined by the length of the depletion region and the dopant concentration. It is quite small, i.e., in the pF region. During the transient switching from off to on, the diode can respond to the applied square wave rapidly without any delay. Under a forward bias, there is additional charge due to excess carriers introduced by the flowing current. During the transient switching from on to off, the voltage across the junction diode doesn't respond to the applied square wave instantaneously. There is a delay.

To see the transient characteristics of a p-n junction diode, revise the voltage source to a square wave as shown below.

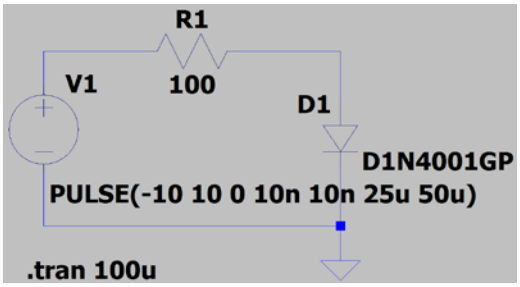


Fig. 5. The circuit to study the transient switching of a diode.

Run the simulation. Plot the input signal and the voltage across the diode as shown below.

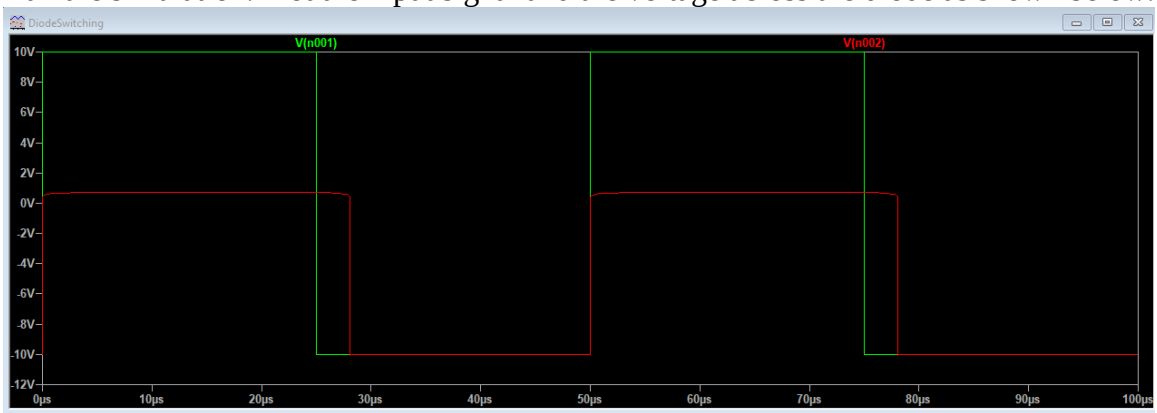


Fig. 6. Transient response of the 1N4001 shown in red to a ±10 V, square-wave input signal shown in green. During the on state, the diode voltage is small, e.g., 0.6 V. There is a delay to switch the diode from on to off. The delay correlates with the current. The higher the current, the longer is the delay.

What is the delay to switch from on to off? (Answer: 3 μsec.) The off-to-on transition, however, is fast. Because of the significant delay, power rectifying diodes are limited to low-frequency operations. Only signal diodes, such as 1N914, with a small junction can rectify radio frequency signals. You can replace 1N4001 by 1N914 and compare the switching delay. You can also change the resistance to find the correlation between the delay and the current.

Diodes can rectify ac signals into dc. The power grid distributes electricity using ac because the voltage can be easily modified by a transformer. To minimize the transmission loss, long haul power lines operate in the 100-750 kV range. Such a high voltage is extremely dangerous. It is down transformed to 117 V or 220 V in several steps before the final distribution to homes. Major appliances operate with ac. High power rated ones, e.g., the central air conditioning system and the electrical car charging system, use 220 V. Low power rated ones use 117 V, e.g., a hair dryer. The ac is converted to dc by a power supply for electronic circuits. A personal computer, for example, operates with 3.3 V or 5 V for logic and 12 V for peripheral. The voltage to run the cpu, however, can be as low as 0.7 V. Even though the voltage is low, cpu can still consume a substantial amount of power. A desktop cpu can draw a current as much as 100 A.

Let's consider the following dc power supply circuit. The circuit consists of four parts, an ac power source, a bridge rectifier, a ripple filter and a regulator IC. The ac power source is represented by a sine wave voltage, *V1*. In the physically implementation, it is a transformer converting from 117 V ac to 12.7 V ac. The ac power source is isolated from the ground. The bridge rectifier consists of four diodes. The negative portion of the ac waveform is inverted to become positive. This is a full wave rectifier.

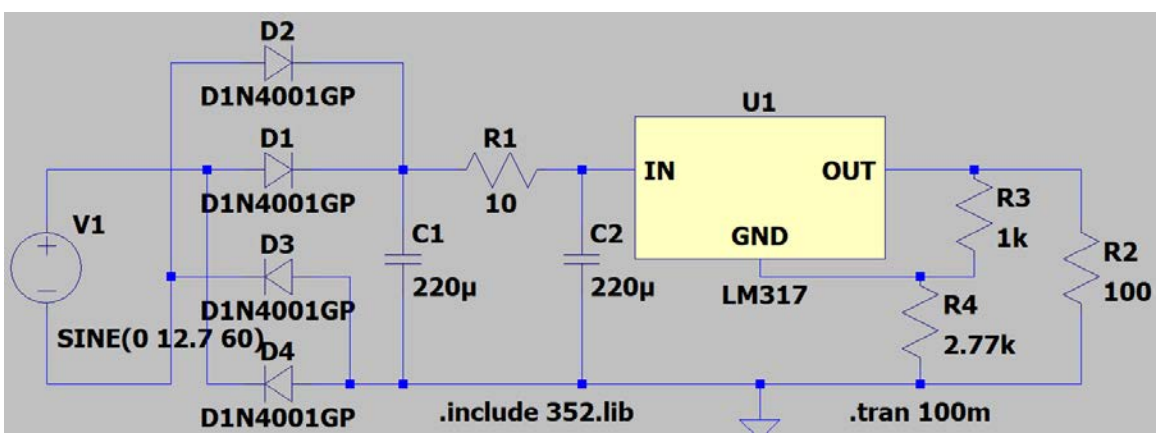


Fig. 7. Regulated dc power supply circuit with a load resistor, R_2, attached.

The output waveform of the full-wave rectifier contains a dc component but is still very much time varying. To reduce the time variation, one can take advantages of low-pass filters. Attach the π-filter consisting of C_1, R_1 and C_2 to the output of the full-wave rectifier. The capacitance should be 100 μF and up. In the actual implementation, one needs to pay close attention to the polarity and the maximum voltage rating of electrolytic capacitors. Over voltage can cause the electrolytic capacitor to explode.

The resistance in the π-filter, R_1, should be small, e.g., 1-10 Ω. It is in series with the load, therefore, the load current flowing through R_1 results in a voltage drop. The voltage drop increases as the load current increases. This loading effect makes the output voltage current dependent. The larger the current, the smaller is the output voltage of the π-filter. You can replace R_1 with an inductor, which has almost no dc loss. While displaying the output waveform, you will observe the ac ripple; especially when the load current is high. The ac ripple reflects the charging of the capacitor by the rectifying diode and discharging by the load resistor. The amount of ac ripple correlates with the load current. The higher the current, the faster the discharge, and the larger is the ac ripple. A large capacitance reduces the ripple.

To reduce the loading effect and ripple, attach a linear regulator IC to the output of the π-filter. Add two resistors, R_3 and R_4, for voltage adjustment as shown in Fig. 4. In real implementation, you can use a 10-kΩ potentiometer as R_4. Start with zero resistance. By increasing R_4, you can increase the output voltage. The ripple should be negligible. When the dc output voltage increases to a certain level, the ac ripple suddenly appears. The regulator IC no longer functions properly. The input voltage needs to be higher than the output for the regulator IC. The minimum voltage difference needed is called the dropout voltage. For LM317, it is around 1.7 V.

Datasheet is an important resource while designing circuits. Information of the LM317 regulator IC is posted at www.ti.com/lit/ds/symlink/lm317.pdf?ts=1630501330515. The device has several variations in packaging with different pin configuration and current, hence, power, handling capabilities. The output voltage can vary from 1.25 V to 37 V. The thermal characteristics provide information to users for choosing the heatsink. The performance of the IC is in the electrical characteristics section. Section 9 is essentially the application note. In it, users can find typical circuits of the IC for various applications. Whenever a new device is considered for circuit implementation, one should always examine the datasheet before designing the circuit.

To get a thorough understanding of the circuit, run simulations in steps. Disconnect both *C1* and *R1*. Run the simulation. Observe the waveform at the output node of the bridge rectifier. You can see that the negative portion of the sine wave is flipped to positive. Reconnect *C1* and *R1*. Run the simulation. You can see the ac ripple at the upper node of *C2*, i.e., the output of the π-filter. What is the peak-to-peak voltage of the ac ripple? You can also see the flat, 5-V dc at the output of the regulator after the initial transient turn-on. The ac ripple decreases when you increase the load resistance, hence, reduce the load current. The ac ripple increases when you decrease the load resistance, hence, increase the load current. Change the load resistance to 30 Ω to substantially increase the load current, hence, the ripple. You start to see a small, transient dip in the output voltage of the regulator IC. The input voltage to the regulator IC is not sufficient to prevent drop out. Set the load resistance back to 100 Ω. You can change R_4 to adjust the output voltage. In simulations nothing will overheat and burn. In real implementations, the load resistor can burn. The electrolytic capacitor can burst due to over voltage.

Here is a summary of what we learn in Chap. 5. The p-n junction diode conducts only in the forward direction. By performing curve fitting, one can determine device parameters. A diode can turn on rapidly. However, there is a delay to turn it off. Power rectifying diodes are used to convert from ac to dc. Using a ripple filter and a regulator IC, one can obtain a very stable dc voltage.

The regulated power supply presented in this chapter has a limited efficiency. Both the resistor in π-filter and the regulator IC, which operates in the linear regime, consume power. It is fine for low-power applications. For high-power applications, a switch mode power supply is preferred. The switch mode power supply has minimal internal power dissipation. It operates at much higher frequency with compact inductors and capacitors. The regulator operates in the switching mode with very little internal power dissipation. The overall efficiency of a switch mode power supply can exceed 90%. However, a switching circuit generates more high-frequency electromagnetic interference (EMI). The switch mode power supply must have EMI filters and be well shielded. An introduction of the switch mode power supply is located at: www.electronics-tutorials.ws/power/switch-mode-power-supply.html.

6. Bipolar Junction Transistor Amplifier

As discussed in Chap. 4, transistors are the building blocks of electronic amplifiers. In a bipolar junction transistor (BJT), a small input current from base to emitter controls a much larger current flowing from collector to emitter. The picture of a 2N3904 BJT and its pin configurations are shown in Fig. 1. It is a npn transistor for small signal applications. Both the collector and emitter are n-type while the base is p-type.

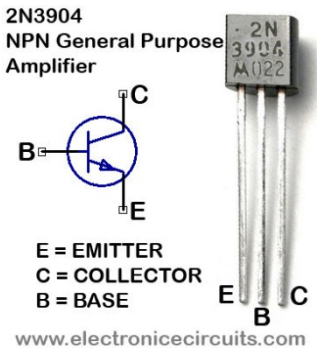


Fig. 1. The pin configuration of a npn BJT. The model is marked on the package.

To learn how to operate a transistor, we need to examine its current versus voltage characteristics. To get the I_C versus V_{CE} characteristics, compose and simulate the circuit shown in Fig. 2. The base current is 20 μA, which can be adjusted. Plot waveforms of V_{CE} and I_C. As discussed in Chap. 3, export the data. Open the data file in Excel. Select the data range. Insert a scatter plot of I_C versus V_{CE}.

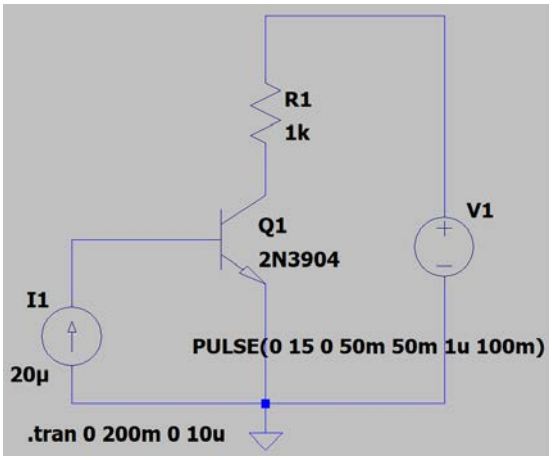


Fig. 2. The circuit diagram for obtaining the I_C versus V_{CE} characteristics in simulations.

By adjusting the current source connected to the base node, you can obtain a series of curves for different base current as shown in Fig. 3.

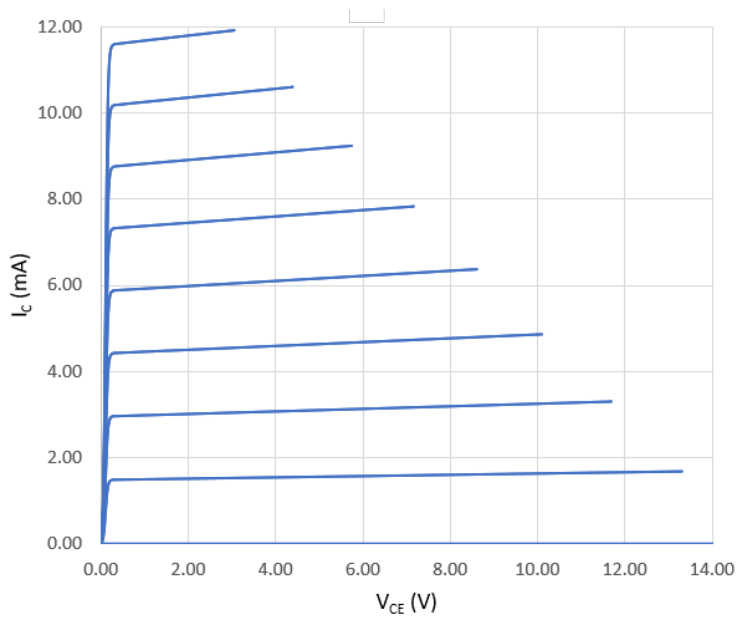


Fig. 3. The collector current versus collector-emitter voltage as a function of base current. The base current of the highest curve is 40 μA. The base current decreases in steps of 5 μA.

The measured device characteristics lead to device parameters. Using the device parameters, one can calculate the amplifier performance. The ratio of the increment in I_C to that of I_B determines the following *h*-parameter:

$$h_{FE} = \frac{\Delta I_C}{\Delta I_B} \quad , \qquad V_{CE}\text{=constant.} \tag{1}$$

When I_B increases from 10 μA to 20 μA, how much does I_C increase? (Answer: approximately 3 mA.) What is h_{FE}? (Answer: 300.) The collector current I_C increases sharply as V_{CE} is increased from zero. As V_{CE} rises above 0.2 V, I_C changes only slightly with V_{CE}. This is the region to operate a BJT linear amplifier. The slope of the plot in this region determines the following *h*-parameter:

$$h_{OE} = \frac{\Delta I_C}{\Delta V_{CE}} \quad , \qquad I_B\text{=constant.} \tag{2}$$

For the curve corresponding to an I_B of 15 μA, what is the slope? (Answer:5.9x10^{-5} Ω^{-1}.)

Similarly, readers can compose and simulate the circuit shown in Fig. 4 to obtain the I_B versus V_{BE} plot.

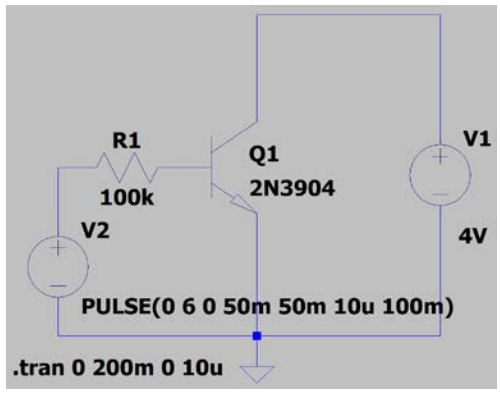


Fig. 4. The circuit diagram for obtaining the I_B versus V_{BE} characteristics.

The input characteristics of the 2N3904 are shown in Fig 5.

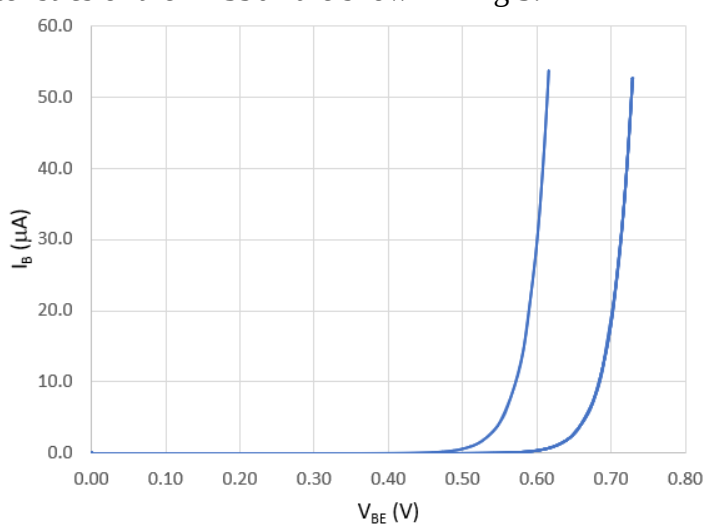


Fig. 5. The input characteristics of BJT with V_{CE} ranging from 0 to 4 V. The first curve is obtained when V_{CE} is zero. Curves taken at a V_{CE} greater than 1 V merge into the second curve.

At any given I_B, one can draw a line tangential to the curve. The inverse of the local slope of this tangential line determines the following parameter:

$$h_{IE} = \frac{\Delta V_{BE}}{\Delta I_B}, \qquad V_{CE}\text{=constant.} \tag{3}$$

The slope changes with I_B. When I_B is at 15 μA, what is the local slope of the curve with a V_{CE} of 4 V? (Answer: approximately 1.6 kΩ.) When I_B is at 5 μA, what is the local slope? (Answer: approximately 6 kΩ.) The value of h_{IE} decreases as I_B increases. There is the fourth *h*-parameter defined as:

$$h_{RE} = \frac{\Delta V_{BE}}{\Delta V_{CE}} \quad , \qquad I_B\text{=constant.} \tag{4}$$

It can be neglected because curves merge into one when V_{CE} is greater than 1 V.

The common-emitter BJT amplifier shown in Fig. 6 represents a transistor amplifier. There are two bias resistors connected to the base node. These resistors are used to provide the required base bias current. The base bias current equals the difference between the current flowing through R_1 and the current flowing through R_2. The resistor R_E is used to stabilize the circuit against variations of device parameters. Of course, it also affects the base voltage. The output is taken from the collector. There are two coupling capacitors, C_1, C_2, and one bypass capacitor, C_E. They limit the low-frequency response of the amplifier. The product of R_E and C_E not only affects the low-frequency response but also determines the time needed to reach the steady state after the amplifier is powered up initially.

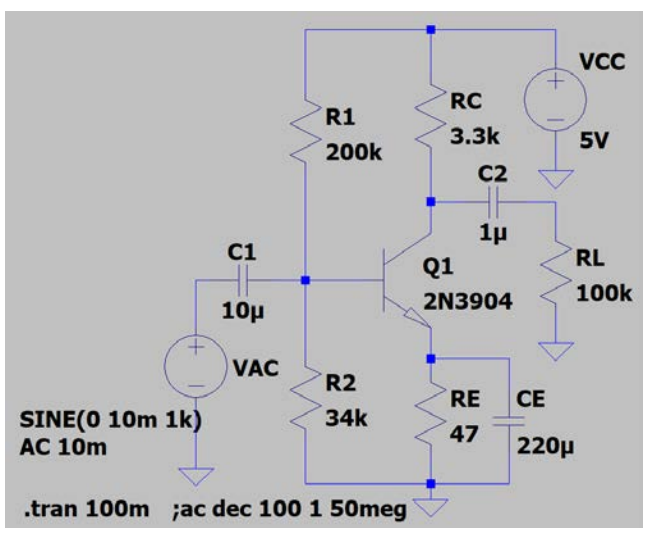


Fig. 6. The schematic diagram of a BJT amplifier in the common-emitter configuration. There are two coupling capacitors, C_1 and C_2, and one bypass capacitor, C_E. The load resistor is R_L.

The h-parameters provide transistor characteristics for the dc and low-frequency analysis. To analyze the ac small-signal gain and the frequency response of the circuit, we need to consider the hybrid-π model shown in Fig. 7. The resistance of the base lead is r_x. The resistance of the base-emitter junction is r_π. The internal collector resistance is r_c. There are two junction capacitors, C_μ and C_π. They both limit the voltage gain at high frequencies. The transconductance is g_m, which has a unit of Ω^{-1}. The unit milli-Ω^{-1} is also called milli-Siemens (mS). The transconductance generates a current proportional to the voltage across r_π.

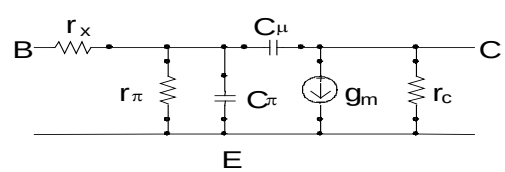


Fig. 7. The hybrid-π model of the BJT.

Based on the ideal diode model for the base-emitter junction and $I_C \cong I_E$, which is linearly proportional to the base current, it can be shown:

$$g_m = I_C \cdot \frac{e}{kT}, \tag{5}$$

where e is the elementary charge and k is the Boltzmann constant. At room temperature with the current in the unit of mA,

$$g_m = 38.9 \cdot I_C \quad \text{mS}. \tag{6}$$

By neglecting r_c at the output and r_x at the input of the hybrid-π model, the voltage gain becomes:

$$A_v = g_m R_C. \tag{7}$$

Since g_m increases as I_C is increased, the gain of the amplifier depends on the bias condition. For the same R_C, the larger the current, the higher is the voltage gain. The gain can only be fully realized for a small input signal. The output waveform is bound by the power supply voltage and the ground. If the input signal is too large, the output will become clipped. Please note that the voltage gain in Eq. (7) doesn't take into account any load

resistance. When a load resistor is attached, the gain will be reduced because of voltage dividing between the load resistance and output impedance of the amplifier.

The h-parameters are related to parameters in the hybrid-π model via the following relations:

$$h_{FE} = g_m r_\pi, \tag{8}$$

$$h_{IE} = r_\pi + r_x, \tag{9}$$

$$h_{OE} = \frac{1}{r_c}. \tag{8}$$

The value of r_x is small, hence, can be neglected. Using numerical values previously found for h_{IE}, h_{FE} and h_{OE}, what are the values of r_π, g_m and r_c? (Answers: 1.6 kΩ, 188 mS and 17 kΩ.) Is the deduced value of g_m close to the ideal model, i.e., Eq. (6)? Please note that these parameters depend on the dc bias conditions.

To design an amplifier, one must first consider design goals, e.g., voltage gain, output peak-to-peak voltage, cutoff frequency, etc. The power supply voltage can limit the gain and the output voltage swing. For a 5-V power supply, keep the design goals modest, i.e., a gain greater than 60, a voltage swing of 2 V. If you use a 15-V power supply, you should set the design goal high, i.e., a gain of 260, an output voltage swing of 8 V. The following procedures can be used to design the dc operating point, i.e., Q-point or bias conditions. The choice made for the circuit shown in Fig. 6 is shown at the end of each step.

1. Select arbitrarily a power supply voltage, V_{CC}, 5-15 V. The power supply voltage must be larger than the desired output voltage swing. (V_{CC} 5 V)
2. Select arbitrarily a moderate R_E, 47-470 Ω, for stabilization. To get a better low-frequency response, pick R_E on the high side. On the other hand, a high R_E can reduce the voltage gain because of reduced current. A large R_E also leads to a large dc voltage at the emitter node. It can cause waveform clipping at the bottom, hence, limit the output voltage swing. Circuit design always involves compromises. If you are using a 5-V power supply, pick 47 Ω. (R_E 47 Ω)
3. You may select I_C. If you choose to operate at a low I_C, the output impedance of the amplifier will be high. On the other hand, at high I_C, the power consumption of the amplifier will be high. A moderate current of 0.5-5 mA is reasonable. Determine V_E from I_E, which is nearly equal to I_C, and R_E using V_E=I_E·R_E. You may also select V_C. If the design goal is to get a large voltage swing without clipping, choose V_C at the mid-point between V_E and V_{CC}, i.e., V_C=(V_{CC}+V_E)/2. If the design goal is to maximize the

gain, choose V_C close to V_E, e.g., V_C=V_E+1.2 V. Calculate R_C from V_{CC}=$I_C \cdot R_C$+V_C. (I_C 0.9 mA, V_C 2 V and R_C 3.3 kΩ)

4. Calculate g_m using Eq. 3, or, more accurately, find g_m from curve tracer plot. (g_m 35)
5. Determine V_B from V_B=V_E+0.65 V. (V_B 0.69 V)
6. Calculate I_B from I_B=I_C/β_{dc}, where β_{dc} is comparable to h_{FE}, i.e., 300. (I_B 3 μA)
7. Pick R_1 to provide sufficiently large bias current for base, $V_{CC}/R_1>I_B$. (R_1 200 kΩ)
8. Calculate R_2 from I_B=(V_{CC}-V_B)/R_1-V_B/R_2. (R_2 37 kΩ)

To analyze the ac input and output impedances, the transistor in the circuit is replaced by its small signal model. Since the power supply behaves like a large capacitor, it is effectively grounded for ac analysis. Based on the small signal model, the input impedance of the common-emitter amplifier is:

$$Z_{in} = (r_x + r_\pi) \| R_B, \tag{11}$$

where R_B=R_1 ‖ R_2. By neglecting r_x, Z_{in} becomes r_π‖ R_B. Since bias resistors are in the few tens to hundred kΩ range, the input impedance is essentially r_π. The output impedance of the amplifier is

$$Z_o = R_C \| r_C. \tag{12}$$

It becomes R_C when r_c is much larger than R_C. The output impedance and the load resistor form a voltage divider. A load resistance comparable to or smaller than the output impedance of the amplifier can and will substantially reduce the voltage gain.

The internal junction capacitances, C_π and C_μ, and the gain of the amplifier determine the high-frequency cutoff. Often, there is a tradeoff. The higher the gain, the lower is the bandwidth. Design procedures discussed here illustrate how to perform the analog circuit design. There is always a compromise in engineering design. You may gain some here and lose some there. As long as all design goals are met, the design with a low cost and high tolerance is the ultimate winner.

Run the transient analysis. Display the input waveform at the base node and the output waveform at the collector node. At the output, the waveform goes through a transient stage reflecting the charging of capacitors. It reaches the steady state quickly. Find the peak-to-peak voltages. Determine the voltage gain. What is the gain? (Answer: approximately 100). To see how the bias condition can affect the gain, revise R_1 to 270 kΩ to lower the bias current. What are the dc and the peak-to-peak ac voltages at the collector node? (Answers: 4.7 V dc and 0.21 V ac.) What is the gain? To see the phase difference between the input

and output waveforms, display waveforms before C_1 and after C_2 to eliminate the dc component. What is the phase difference? (Answer: 180^0.) Go back to display the waveform at the collector node. What do you expect when you increase the amplitude of the waveform generator to 50 mV? (Answer: Waveform heavily rounded neat the V_{CC} voltage.) Set R_1 to 180 kΩ to increase the bias current. What do you observe? (Answer: Waveform clipped at the bottom.) Reduce the amplitude of the waveform generator to 0.5 mV. What is the gain? (Answer: 150.) From these observations, readers can summarize the findings. How does the bias current affect the gain, the dc collector voltage and the waveform clipping? If you notice clipping at the bottom of the waveform, what will you do to avoid it? If you need a higher gain, do you increase or decrease the bias current? Such knowledge will help you to become proficient in circuit design.

Go back to the original settings. Run the transient analysis. To find the output impedance of the BJT amplifier, measure the peak-to-peak voltage, V_{NoLoad}, when there is no load, i.e., R_5 in the circuit diagram is removed. Attach and reduce R_5 until the output voltage is reduced by 10% to 20%. From the load resistance and the reduced output, V_{out}, one can use the voltage divider formula, $V_{out}=V_{NoLoad}\cdot R_L/(Z_o+R_L)$, to derive the output impedance, Z_o. What is the output impedance? Is it comparable to R_C?

The linearity is also an important characteristic of an amplifier. A linear circuit can amplify without introducing any waveform distortion in the time domain. In the frequency domain, a linear amplifier generates no harmonics. In other words, for a sine wave input at 1 kHz, there is no 2 kHz, 3 kHz, etc. present at the output. Nonlinearity starts to show only when the output signal becomes large. As the signal becomes large, the gain of the amplifier saturates. The output waveform of the amplifier becomes distorted and higher order harmonics starts to appear. Revise the circuit diagram by changing R_3 to 220 kΩ and the amplitude of the waveform generator to 30 mV. Run the transient analysis. Display the output waveform. In LTspice, highlight the frame of the waveform display pane. Right click on the waveform and select View, FFT (fast Fourier transform). Select the output node. The spectrum appears. You can see peaks at 1 kHz, 2 kHz, 3 kHz, etc. The vertical axis is in the logarithmic scale. The peak of the spectrum reflects the power, i.e., $20\cdot\log_{10}(V_{\mathrm{RMS}})$, where V_{RMS} is the root-mean-square amplitude. The second harmonic at 2 kHz is -8.5 dB below the fundamental peak at 1 kHz. The third harmonic at 3 kHz is -21 dB below the fundamental peak. By reducing the input amplitude to 3 mV, the second harmonic is -30 dB below the fundamental peak. It is important to limit the input to ensure that any requirement on linearity or limit on the harmonic distortion is met.

Now, we shift the focus to the frequency domain by running the ac analysis. Display the Bode plot at the output node, i.e., the collector. What is the -3 dB frequency at low frequency? Decrease the capacitance of C_E by a factor of ten. What is the -3 dB frequency? To enhance the low-frequency response, one can increase capacitances of coupling and bypass capacitors. The junction capacitances, notably, C_μ, limit the high-frequency response. By using a smaller R_C, the high-frequency response can be enhanced at the expense of the gain. Most amplifiers behave this way. The higher the gain, the lower is the high-frequency cutoff. There is a figure of merit called the gain-bandwidth product.

hThe common-emitter amplifier has a low input impedance in the kΩ range. Its output impedance is comparable to R_C. If the load resistance is low, the output voltage will decrease. A different circuit, the common-collector amplifier, can provide a very low output impedance. The common-collector amplifier is shown in Fig. 8. Similar to other BJT amplifiers, it has a bias network to provide the base current. The collector is connected directly or through a small resistance to the power supply. There is a resistor between emitter and ground. There is no bypass capacitor. The output is derived from the emitter. Since the base-emitter junction behaves like a forwardly biased diode, the ac output signal at the emitter is almost identical to the input signal at the base. The voltage gain is nearly unity. However, a small ac base current can lead to a large ac current flowing through the load. There is a large current gain. The common-collector amplifier is also referred to as an emitter follower.

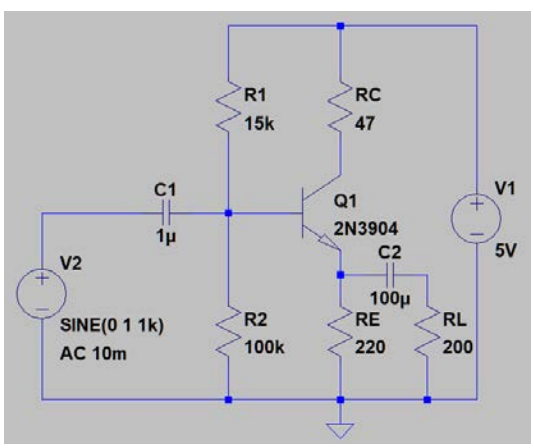


Fig. 8. The common-collector amplifier.

The third BJT amplifier configuration is the common-base amplifier. Its characteristics are similar to those of the common-emitter configuration. It provides a better high-

frequency response. Amplifiers can also be built using pnp BJTs. The polarity or orientation of the power supply, however, needs to be reversed. The current flows from emitter though the base to the collector.

Some logic circuits are BJT based. The circuit shown in Fig. 9 is a resistor-transistor logic (RTL) inverter. The input is a clock signal with two voltage levels, 0 and 5 V, corresponding to logic L and H. Readers can run simulations. Display the input and output signals along with the base current. The response speed is the primary concern of logic circuits. Readers can adjust the base resistor to see how it affects the delay, rise time and fall time of the inverter.

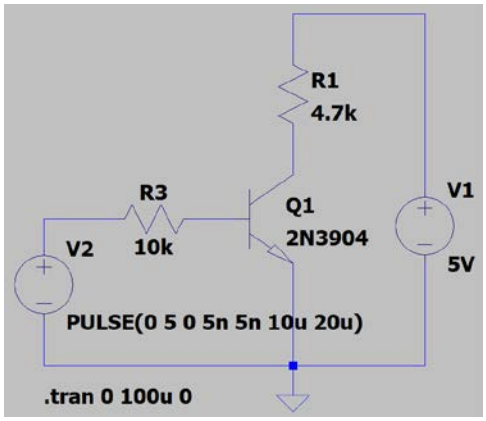


Fig. 9. The resistor-transistor logic inverter.

In summary, BJT is a building block of amplifiers. A BJT can amplify a small input base current to become a large collector current. When the output is taken from the collector node, there is a large voltage gain. When the output is taken from the emitter node, there is a substantial current gain. In order to amplify the input signal linearly, one must operate the amplifier with a proper dc bias and limit the amplitude of the input signal. The frequency response of the BJT amplifier is limited by capacitors, both external and internal. There are various amplifier configurations with different characteristics, e.g., input impedance, output impedance and gain, for different applications.

7. Field-Effect Transistor Amplifier

The purpose of this chapter is to learn characteristics of the field-effect transistor (FET) and how to operate an FET amplifier.

An FET has three terminals, namely, source, gate and drain. There is a conducting channel between the source and drain to carry the current. The channel can be n-type or p-type. The flow of carriers from the source to the drain is controlled by an externally applied voltage at the gate. The gate voltage creates an electrical field either through a reversely biased p-n junction (JFET) or a metal-oxide-semiconductor junction (MOSFET). The electric field regulates the channel, hence, controls the current. The device, 2N3819, is a JFET. Shown below is the pin configuration reproduced from the manufacturer's datasheet of 2N3819.

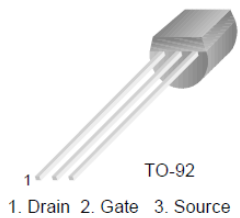


Fig. 1. The pin configuration of 2N3819 JFET.

To get the I_D versus V_{DS} characteristics, compose and simulate the circuit shown in Fig. 2. Please note that 2N3819 operates with a negative gate voltage.

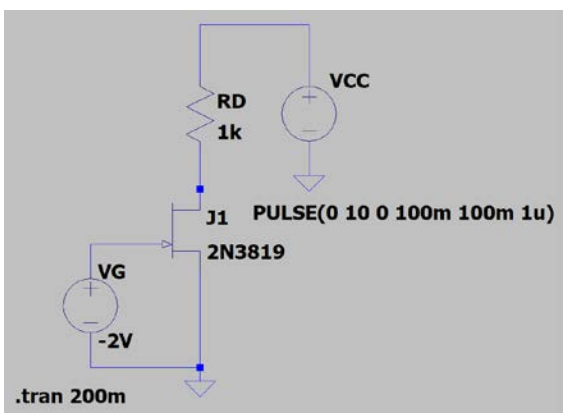


Fig. 2. The circuit diagram for obtaining the I_D versus V_{DS} characteristics.

Plot waveforms of V_{DS} and I_D. Export the data. Open the data file in Excel. Select the data. Insert a scatter plot. By adjusting the voltage source connected to the gate node, you

can obtain a series of curves as shown in Fig. 3. The region in which curves rise quickly is called the triode region. The region in which curves are flat is called the saturation region. This is the region to operate a linear amplifier. Compare this plot to the I_C versus V_{CE} plot of the 2N3904 BJT. What is the main difference? The curve of FET is slow to become flat. A larger V_{DS} is needed to operate a linear FET amplifier.

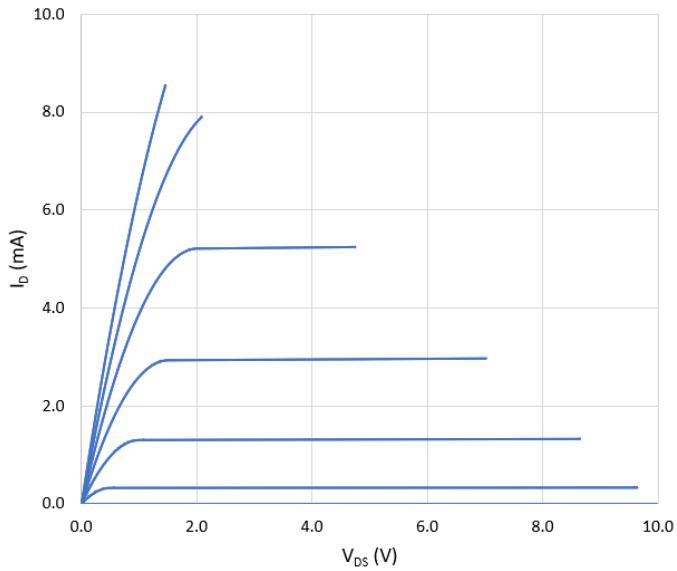


Fig. 3. The drain current versus drain-source voltage as a function of gate voltage. The gate voltage of the highest curve is 0 V. The gate voltage becomes increasingly more negative in steps of -0.5 V.

The small-signal model of the FET at low frequency is shown in Fig. 4.

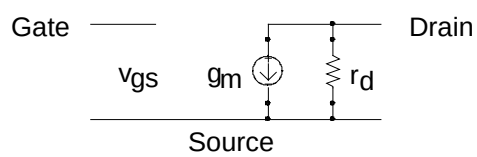


Fig. 4. The small-signal, equivalent circuit of an FET.

The resistance between the gate and the source is essentially infinity, i.e., an open circuit. An ac signal, v_{gs}, is applied between the gate and the source. It creates an ac current flowing between drain and source. The current is proportional to the transconductance, g_m. There is an internal drain resistance, r_d, between the drain and the source. These parameters can be determined from curves shown in Fig. 3.

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}, \qquad V_{DS}\text{=constant.} \tag{1}$$

$$r_d = \frac{\Delta V_{DS}}{\Delta I_D}, \qquad V_{GS}\text{=constant.} \tag{2}$$

Since curves in Fig. 3 are not evenly spaced, g_m is clearly not a constant. It is a function of V_{GS}, hence, I_D. A larger I_D leads to a higher g_m. What is g_m for a gate voltage of -1.5 V? (Answer: approximately 3.3 mS^{-1}.) What is r_d? (Answer: essentially infinity.)

To get the I_D versus V_{GS} characteristics, compose and simulate the circuit shown in Fig. 5.

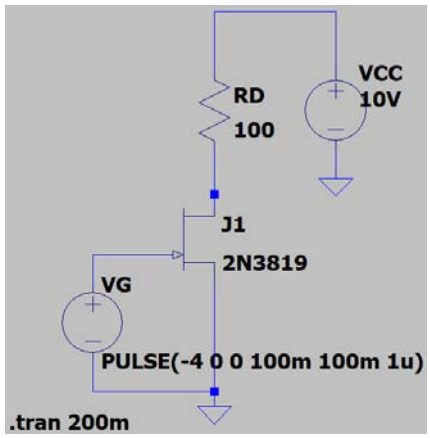


Fig. 5. The circuit to determine the drain current versus the gate-source voltage.

After running the simulation, display the gate voltage and drain current. Save the data, use Excel to open the file and plot the data as shown in Fig. 6.

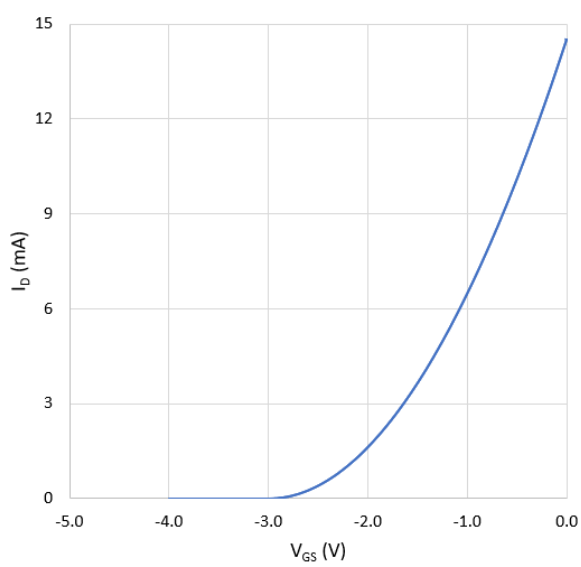


Fig. 6. The drain current versus gate-source voltage.

When V_{GS} is below the pinch-off voltage, V_P, there is no current. What is V_P? (Answer: -3 V.) The curve of I_D versus V_{GS} above pinch off can be fitted with the following parabolic equation:

$$I_D = \frac{I_{DSS}}{V_P^2} \cdot (V_{GS} - V_P)^2 \tag{3}$$

What is I_{DSS}? (Answer: 14.5 mA.)

The circuit diagram of a JFET amplifier in the common-source configuration is shown in Fig. 7.

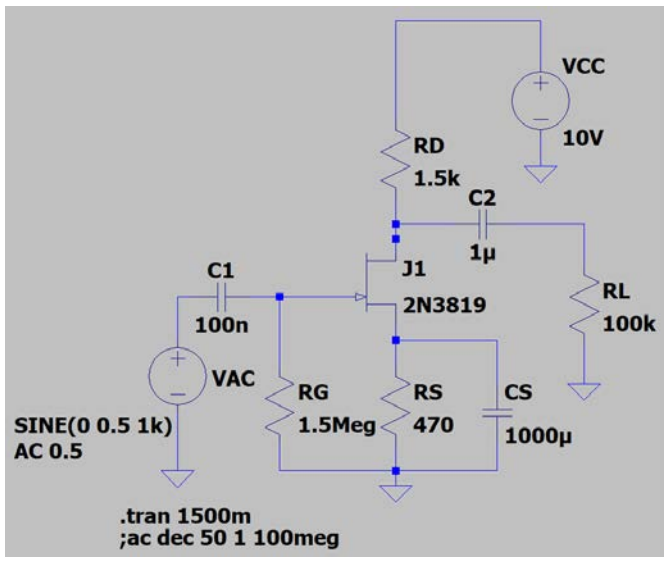


Fig. 7. The schematic diagram of the common-source JFET amplifier.

The n-channel JFET requires a negative bias voltage at the gate. Since there is no dc current in R_G, the dc voltage at the gate is zero. The dc current flowing through R_S sets up a positive dc voltage at the source node. As a result, there is a negative gate-to-source bias. The dc gate voltage determines the dc drain current. The ac input signal is connected to the gate via a coupling capacitor. The drain is the output node. Based on the small-signal equivalent circuit, the voltage gain is given by

$$A_v = -g_m \cdot (R_D \parallel r_d). \tag{4}$$

The negative sign indicates a 180° phase reversal between the output and input. The output impedance is determined by R_D and r_d in parallel. Since the gate impedance of FET is very high, the input impedance of the amplifier is determined by R_G. A load resistor can be

attached through a coupling capacitor to the drain node. The output impedance and the load resistor form a voltage divider. The voltage across the load will decrease, hence, the gain will drop, when the load resistance becomes comparable to R_D.

Run the transient analysis. From the waveforms at various nodes, determine the drain node dc voltage and the ac peak-to-peak voltage, the source node dc voltage, the gate node dc voltage and the drain node dc current. What is the dc V_{GS}? (Answer: -1.47 V.) What is the dc V_{DS}? (Answer: approximately 3.9 V.) What is the dc I_D? (3.2 mA.) The dc V_{DS} and I_D define the Q (quiescent) point in the I_D versus V_{DS} plot. Does the Q-point sit in the region where curves are flat? What is the ac voltage gain? (Answer: 5.) In comparison with the BJT amplifier in the common-emitter configuration, the voltage gain of the FET amplifier is much lower because of the low transconductance.

Similar to the BJT amplifier, the frequency response of the amplifier is determined by *RC* time constants in the circuit. The coupling capacitor at the input and the input impedance of the circuit form a high-pass filter. The output impedance, output coupling capacitor and the load resistance form another high-pass filter. The third low-pass filter is formed by R_S and C_S. They all limit the low-frequency response. Is there a low-pass filter limiting the high-frequency response? Indeed, there is. The high-frequency limit is determined by the junction capacitance of the FET and R_D. Run the ac analysis. From the Bode plot, determine the -3 dB cutoff points at low and high frequencies.

After finding the nominal characteristics of the circuit, we can explore the circuit design by making modifications. According to Eq. (4), the gain can be reduced by using a smaller R_D. Can the gain be increased by making R_D or I_D larger? The answer is yes but with a limitation. When you increase R_D, V_{DS} decreases. Eventually, the Q-point moves from the saturation region into the triode region. Eq. (4) is no longer applicable. To use a larger R_D, one needs to increase the power supply voltage. How R_S affects the gain and peak-to-peak voltage swing without clipping is left to the readers to explore. When you design and operate a linear FET amplifier, make sure that the Q-point is in the saturation region.

In conclusion, this chapter covers FET characteristics and how to operate an amplifier in the common-source configuration. Due to the high input impedance, FET amplifiers are the choice for applications involving high impedance sources. For example, the front-end amplifier of biomedical instruments is FET-based .

8. Operational Amplifier and Active Filters

Operational amplifier is also a building block, but a very sophisticated one, for electronics. An operational amplifier contains dozens of transistors. They are designed and integrated together to offer high performance. In this chapter, we discuss characteristics of operational amplifiers and learn how to design circuits using operational amplifiers.

Electronic amplifiers can boost weak signals. Basic characteristics of an amplifier include the gain or amplification factor, input impedance or loading to the signal source and output impedance or ability to drive the load. Operational amplifiers are nearly ideal. They offer a high input impedance, a large gain and a low output impedance. These characteristics greatly simplify the task of circuit design. They are much more convenient to use than discrete transistors.

One of the following operational amplifiers, μA741, OP27 or OP37, can be used to study characteristics of operational amplifiers. In the manufacturer's datasheet, the following information can be found. As shown in Fig.1, pin 1 is next to the notch in a dual inline package (DIP) device. Pins are counted in the counter-clockwise direction. Pin 2 is the inverting input. Pin 3 is the non-inverting input. Pin 4 is the negative power supply. Pin 7 is the positive power supply. Pin 6 is the output. Pins 1 and 5 of 741 or pins 1 and 8 of OP27 are for offset adjustment. Pin 8 in 741 or pin 5 in OP27 is not connected. The maximum output voltage, i.e., the saturation voltage, is approximately 0.1 to 1 V below the power supply voltage. The power supply voltage can be ±5 V to ±15 V. The typical output short-circuit current is 40 mA. The typical slew rate, i.e., how fast the output voltage can change, is 0.5-2 V/μsec.

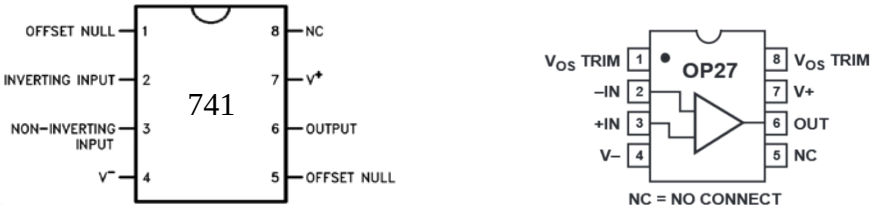


Fig. 1. The pin diagrams of 741 and OP27 operational amplifiers.

Reader can find the circuit diagram inside of LM741 made by Texas Instrument. The file is located in LTspice XVII\examples\Education.

The symbol of an operational amplifier is shown in Fig. 2.

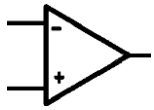


Fig. 2. The symbol of an operational amplifier.

It has two input ports. One is the inverting input (V_{-IN}), i.e., the output signal is 180° out of phase with respect to the signal at this input node. The other is the non-inverting input (V_{+IN}). The open-loop gain, A, of a typical operational amplifier is large, i.e., >1000. It is internally compensated and short-circuit protected. It has an excellent stability, therefore, is free from any self-oscillation. For dc input, a dual voltage power supply with both positive and negative voltages should be used. The common node of the dual voltage power supply is connected to the circuit ground. For ac coupling, a single positive power supply is sufficient.

The output voltage, V_o, is related to the difference of voltages at the input.

$$V_o = A \cdot (V_{+IN} - V_{-IN}). \tag{1}$$

This is the differential gain. When two input voltages are the same, the common-mode gain is negligibly small. When there is no feedback loop from the output to the input, because of the large open-loop gain, a small input can drive the operational amplifier into saturation. A sine wave input can generate a square or trapezoidal wave at the output. Readers can simulate the circuit shown in Fig. 3 to find the saturation voltage. How far is the saturation voltage from the power supply voltage? (Answer: 0.5 V). In real devices, there may be a small difference between positive and negative saturation voltages.

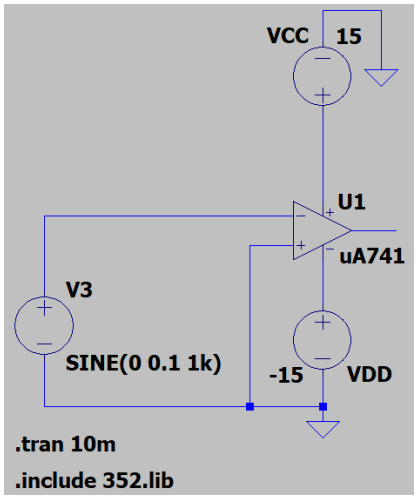


Fig. 3. The circuit diagram for finding the saturation voltage.

In additional to the limit on the maximum output voltage, there is also a limit on how fast the output voltage can change. The maximum rate of change is called the slew rate. To find the slew rate, readers can simulate the buffer amplifier with unity gain shown in Fig. 4. The input is a square wave. After running simulations, readers will find that the output is a trapezoidal signal. The slope of the rising edge and the trailing edge is finite. What is the slew rate? (Answer: 0.5 V/μsec).

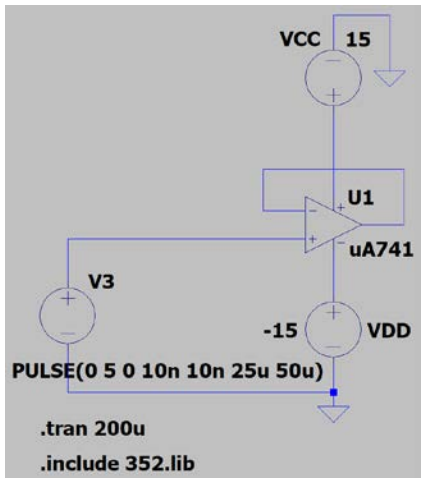


Fig. 4. The circuit diagram for finding the slew rate.

When a feedback resistor is connected from the output to the inverting input, the operational amplifier is intended for linear amplification. An example of a simple inverting amplifier is shown in Fig. 5. Since the input impedance of the operational amplifier is very large, any current provided by the signal source must flow through the feedback resistor, R_2. In addition, the open-loop gain is very large. Therefore, the voltage difference between two input ports must be nearly zero. Since the non-inverting input is connected to the ground, the inverting input port is virtually grounded. From the current flow, one can easily find the voltage gain, which is the ratio of the output voltage to that of the input voltage provided by the waveform generator, V_o/V_{in}.

$$A_v = -R_2/R_1. \tag{2}$$

The negative sign simply indicates that there is a 180° phase shift between the input and output signals. A positive input voltage is amplified to become a negative output voltage.

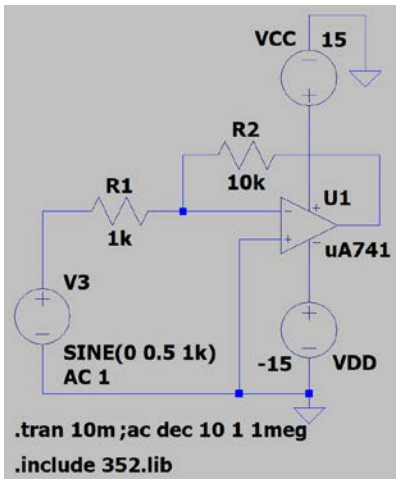


Fig. 5. A simple operational amplifier circuit with pin 7 connected to the positive V_{CC} and pin 4 to the negative V_{DD}. Input signal is connected through R_1 to pin 2, i.e., the inverting input. The output signal has an opposite polarity to the input signal, i.e., there is a phase shift of 180°.

The input impedance of an operational amplifier is large but not infinite. The output impedance is low but non-zero. Therefore, resistors in the range of kΩ to a few hundred k Ω should be used in constructing the amplifier circuit. Otherwise, assumptions used in deriving the voltage gain become invalid. What is the gain for the circuit shown in Fig. 5? (Answer: -10). Perform the ac analysis to obtain the Bode plot, i.e., the frequency response. What is the -3 dB frequency? (Answer: 72 kHz). By changing R_2 to 100 kΩ what is the gain? (-100). What is the -3 dB frequency for a gain of -100? (Answer: 10 kHz). This is another example that the higher the gain, the lower is the high-frequency cutoff.

Operational amplifiers do deviate from the ideal amplifier. At the input, there are input offset, common-mode input resistance, differential input resistance and input bias current. At the output, there is the current driving capability. The open-loop differential gain, *A*, is large but finite. It also drops off as the frequency is increased. The common-mode gain is small but not exactly zero. The current driving capability can be found in simulations. Attach a 100-kΩ load resistor to the operational amplifier circuit shown in Fig. 5. Reduce the load resistance until the tip of the sine wave output starts to clip. The amplitude of the clipped output signal divided by the load resistance is the current driving capability. What is the current driving capability of 741? (Answer: 40 mA). The common-mode gain of this circuit can also be found in simulations. Rewire the non-inverting input. Connect it to the inverting input. When the input amplitude is 0.1 V, what is the output peak-to-peak

voltage? (Answer: 6 mV). The ratio between the differential mode gain and the common-mode gain is the common-mode rejection ratio. In real devices, there may still be an output when the differential input is zero. This offset can be nulled by connecting two end pins of a potentiometer to the offset adjustment pins of the operational amplifier. Connect the center wiper pin to the negative power supply. Adjust the potentiometer until the output offset is zero.

An operational amplifier can also be configured to amplify without a phase reversal. The circuit diagram is shown in Fig. 6. The input is connected to the non-inverting input. Using the virtual ground concept, one can derive the voltage gain as:

$$A_v = (R_1 + R_2)/R_1. \tag{3}$$

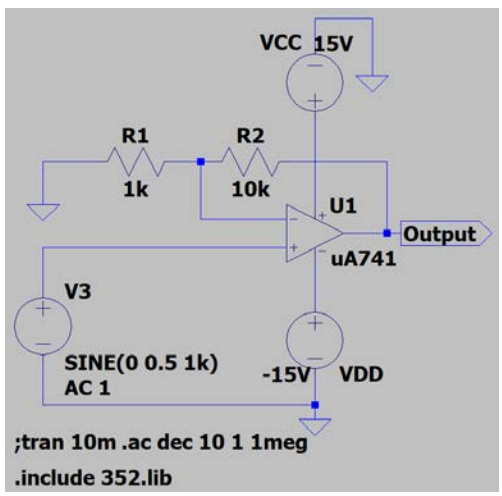


Fig. 6. The circuit diagram of a non-inverting operational amplifier.

Furthermore, an operational amplifier can perform the addition of two or more signals. The diagram of a summing amplifier is shown in Fig. 7. There are two input signals. Each voltage source generates a current. The total current flowing through R_2 generates the output signal. The output signal is proportional to the sum of two input signals but with a negative sign. Run the simulation. Display the two input waveforms and the output waveform. Can you design an operational amplifier circuit to perform the subtraction of two input signals?

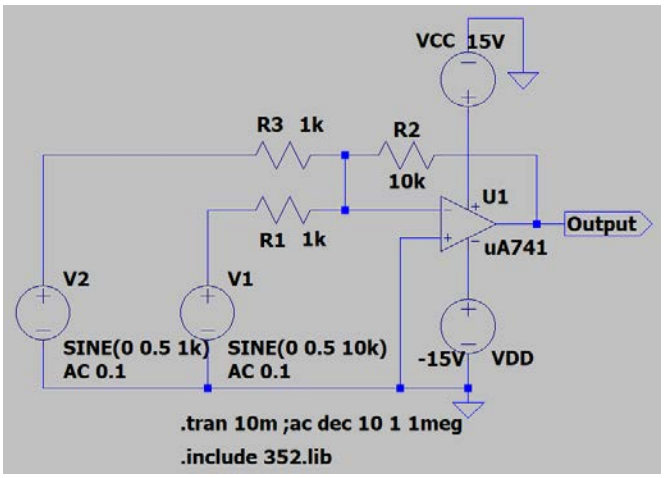


Fig. 7. The circuit diagram of a summing operational amplifier.

Many operational amplifiers can work with only a single power supply. However, a dc reference at half the power supply voltage and ac coupling through a capacitor are needed. The circuit diagram is shown in Fig. 8. The dc reference can be obtained from a simple voltage divider. At the input, R_1 and C_1 form a high-pass filter circuit. There is a low-frequency cutoff.

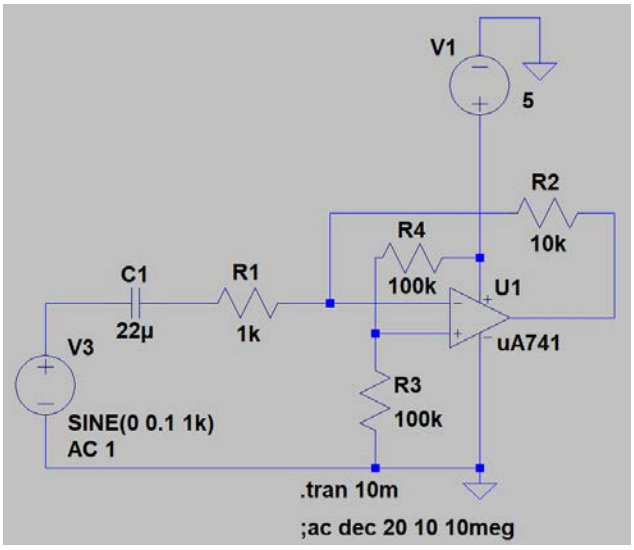


Fig. 8. The ac coupled operational amplifier circuit using a single polarity power supply. The power supply voltage can be as low as +5 V.

Filters are widely used in electronics. They can control the bandwidth, hence, reject noise outside of the signal band. Using operational amplifiers, one can design active filters. Active filters can provide a gain, drive the load, and facilitate sophisticated high-order

filters with sharp frequency responses and high Q values. There are active low-pass, high-pass, band-pass, notch and band-reject filters. Texas Instruments (TI), a manufacturer of operational amplifiers and other electronic components, provides application notes and design references for operation amplifiers. Chapter 16 in "Op Amps for Everyone," Ron Mancini, Editor in Chief, SLOD006B, August 2002 is dedicated to the active filter design. Readers can also find "Filter Design in Thirty Seconds," Bruce Carter, SLOA093, December 2001 on TI website: http://www.ti.com/lit/an/sloa093/sloa093.pdf. In it, you can find circuit diagrams and design procedures for essentially all types of active filters.

For comparison, two low-pass active filters are presented below. The circuit diagram of the first-order, low-pass active filter is shown in Fig. 9. In the circuit, R_1 and C_1 form an integrator. To cap the gain at dc, R_2 is incorporated in the feedback loop.

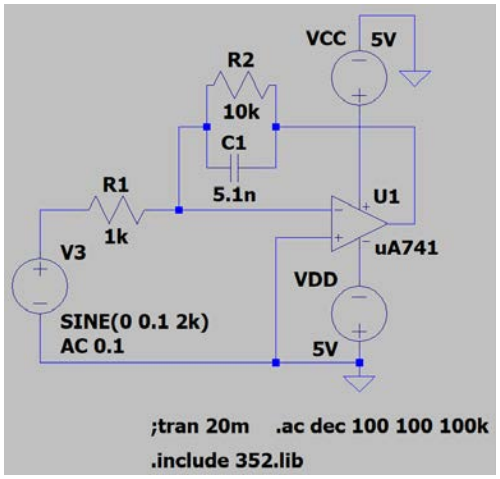


Fig. 9. The circuit diagram of a first-order low-pass filter.

Its Bode plot is shown in Fig. 10.

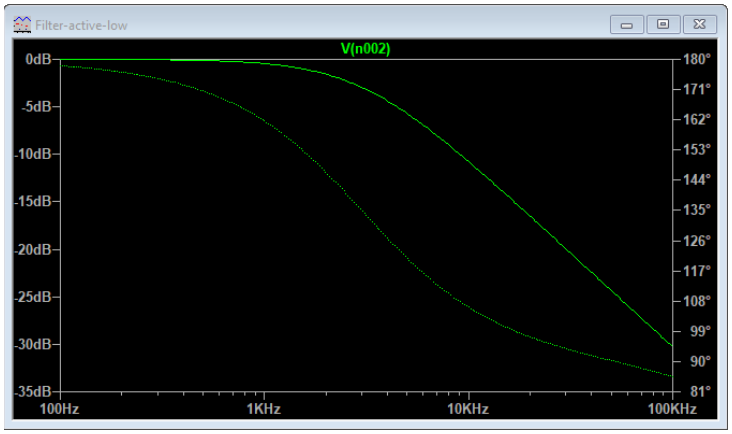


Fig. 10. The Bode plot of the first-order low-pass filter with a -3 dB frequency of 3 kHz.

The circuit diagram of a second-order low-pass active filter is shown in Fig. 11.

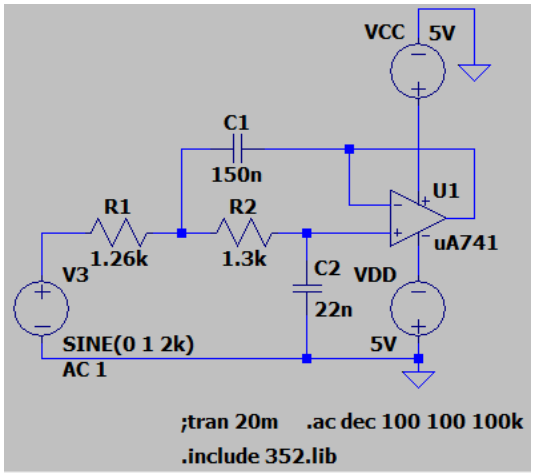


Fig. 11. The circuit diagram of a second-order low-pass filter.

Its Bode plot is shown in Fig. 12.

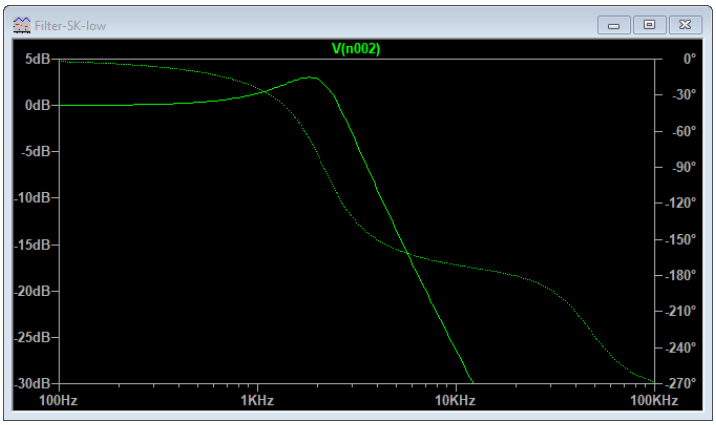


Fig. 12. The Bode plot of the second-order low-pass filter with a -3 dB frequency of 3 kHz.

The second-order active filter has a much sharper roll off beyond 3 kHz. It also has a ripple in the pass band. By cascading the first and second order filters, one can obtain third and higher order filters.

The use of operational amplifiers extends into the digital realm. When noise is present, a decision circuit is needed to quantize the signal into either logic H or L. The level comparator circuit shown in Fig. 13 is an example. In this example, the decision level is set at half of the power supply voltage. The input signal shown in green contains a significant amount noise. When the input is above 2.5 V, the output is H. When the input is below 2.5 V, the output is L. The output signal shown in red is noise free.

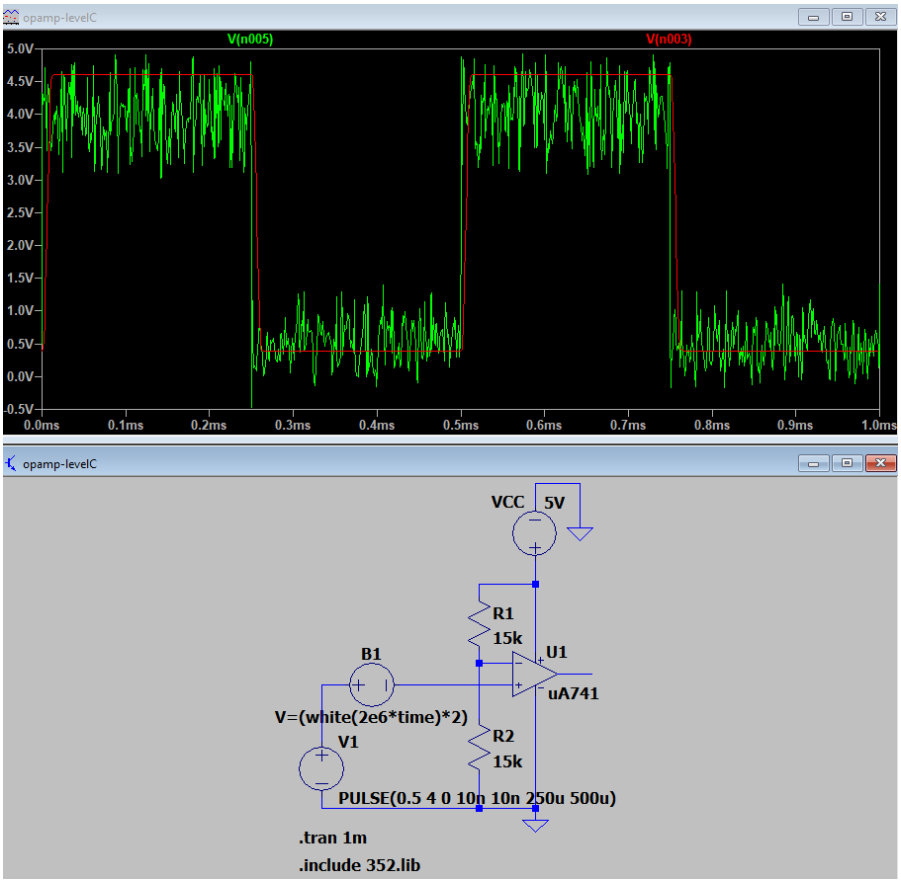


Fig. 13. A level comparator circuit. The second signal source, B1, represents the noise. The noisy input signal is shown in green. The output of the comparator circuit is shown in red.

In this chapter, we learn the basic characteristics, such as the saturation voltage, slew rate and current driving capability, of an operational amplifier. We learn how to build amplifiers and the gain-bandwidth correlation. We also learn how to build active filters and the level comparator.

9. CMOS Logic Gates

Logic gates are the building blocks for computers, digital signal processing systems, digital communications systems, programmable logic controllers and networking systems. In this chapter, we will learn how to use MOSFETs to construct a CMOS inverter, its static and dynamic responses.

Basic logic gates include AND, OR, NAND, NOR, exclusive OR (XOR), buffer, inverter, etc. Their logic symbols and truth tables are covered in digital logic courses. In a field-programmable gate array, there are millions of configurable logic gates. They can carry out sophisticated, application-specific operations. Logic gates developed over the years are categorized according to their physical structures into transistor logic, including low-power Schottky (LS) devices, emitter-coupled logic (ECL), complementary metal-oxide-semiconductor (CMOS) and high-speed, low-voltage, advanced versions. CMOS operates with a very low power consumption. It is the fundamental building block of very large-scale integrated circuits.

The CD4007 chip is a MOSFET array designed for digital switching. Its configuration is shown in Fig. 1. There are three n-MOS and three p-MOS devices in the dual-in-line package (DIP). For p-MOS, source nodes are located at pins 14, 2, 11; drain nodes at pins 13, 1, 12. For n-MOS, source nodes are located at pins 7, 4, 9; drain nodes at 8, 5, 12. Gate nodes are at pins 6, 3, 10. Each gate node is shared by one pair of n-MOS and p-MOS.

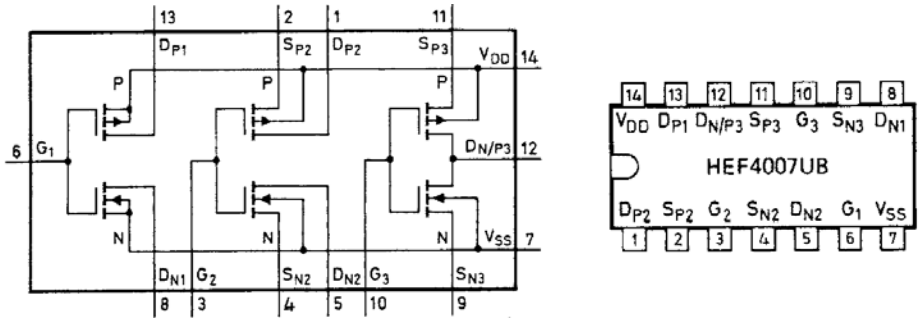


Fig. 1. The schematic diagram and the pin configuration of CD4007.

Digital circuits perform logic operations. We use high (H) to represent logic “1” and low (L) to represent ‘0”. Shown in Fig. 2, is a CMOS inverter consisting of one n-channel and one p-channel MOSFET with the drain nodes tied together as the output. The two gate nodes are also tied together as the input. As the input switches from L to H, the p-channel MOSFET switches off while the n-channel MOSFET switches on, hence, the output

switches from H to L. When the input switches from H to L, the n-channel MOSFET switches off while the p-channel MOSFET switches on. The two MOSFETs are in series and one of them is in the off state. There is no current, hence, no power consumption during the steady state. A transient current, however, does flow during switching. There is a small power consumption. The faster the switching rate, the higher is the power consumption. Therefore, a faster central processing unit (cpu) requires a better cooling solution. One can extend the battery of a notebook computer by slowing down its cpu.

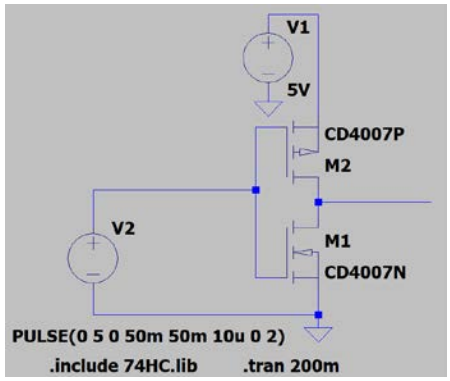


Fig. 2. The schematic diagram of the CMOS inverter. To obtain the static transfer function, a 100-msec triangular wave is used as the signal source. To study the switching characteristics, a 2-MHz clock signal is used.

The static transfer function showing the output voltage versus the input voltage is shown in Fig. 3. Switching takes place when the input voltage is slightly above 2.5 V.

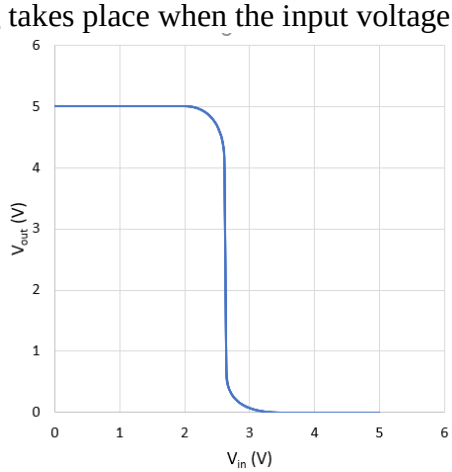


Fig. 3. Transfer function of the CMOS inverter.

Timing is crucial for digital logic operations. The delay is defined as the time difference between the 50% point of input signal and that of the output. The speed of switching is characterized by the rise time from the 10% point to the 90% point of the

output waveform and the fall time from 90% to 10%. They are important characteristics for digital circuits. The switching speed varies among different types of logic gates. Results of simulation are presented in Fig. 4.

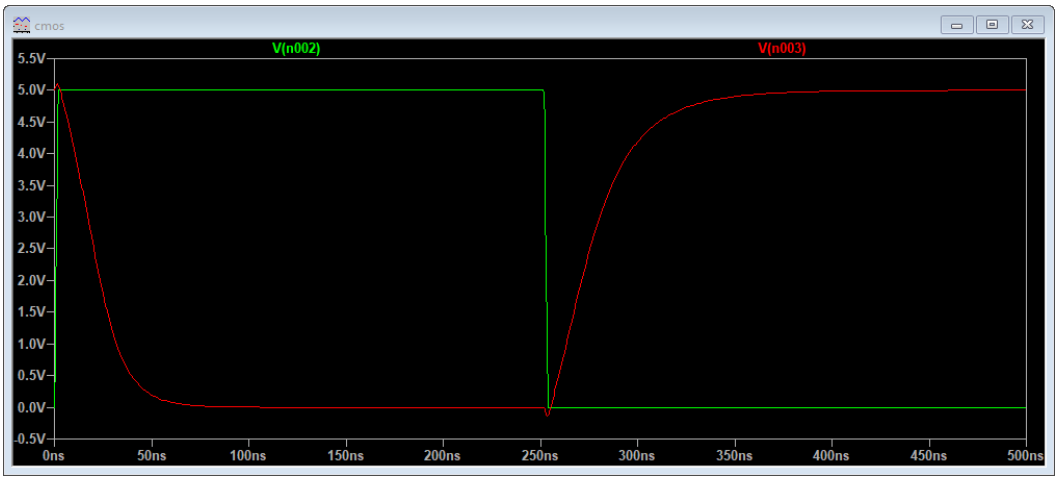


Fig. 4. Transient switching waveforms of the CMOS inverter. The input is shown in green. The output is shown in red.

What is the delay time? (Answer: 22 nsec). What is the rise time? (Answer: 50 nsec). What is the fall time? (Answer: 32 nsec).

When there is a current drawn from a logic gate at H, its output voltage decreases. If the voltage decreases too much, the logic state is no longer valid. The number of logic gates which can be driven by the output is the fan-out capability. It is also an important parameter to consider while designing digital systems. Readers can explore the fan-out capability by adding a load resistor between the output of the CMOS inverter and the ground. Start with 1 MΩ. Gradually reduce the resistance until the output voltage falls below 4 V for logic H. Likewise, readers can connect the load resistor between the output and the positive power supply to find the resistance which can cause the output L to rise above 0.5 V.

Like CD4007, 74HC14 contains inverters but of the Schmitt trigger type. It responds to the input voltage differently. CMOS inverter switches when the input voltage is around 2.5 V. The switching voltage remains nearly constant no matter whether it is a positive transition, i.e., from L to H, or a negative transition, i.e., H to L. The positive switching voltage of 74HC14 is different from the negative switching voltage. In the transfer function plot there is a hysteresis loop as shown in Fig. 5. The graph is cited from the manufacturer's datasheet. The hysteresis loop makes the Schmitt trigger inverter less susceptible to noise.

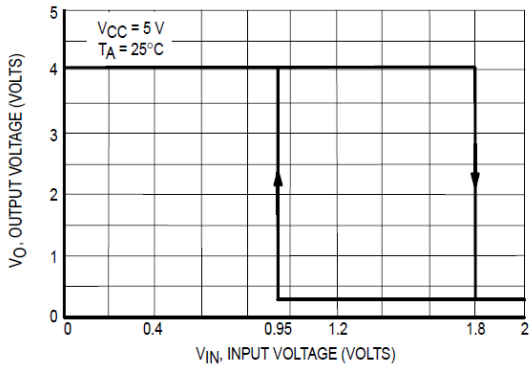


Fig. 5. Transfer function of a typical Schmitt trigger inverter. Switching takes place at a lower voltage than the CMOS inverter and there is hysteresis.

Using the Schmitt trigger inverter, the circuit shown in Fig. 6 can generate a digital signal synchronized to an analog input. A sinusoidal signal with a peak-to-peak voltage around 2 V is connected through a coupling capacitor to the gate of the CMOS inverter. The inverter is dc biased near its switching point. The positive portion of a sine wave drives the output of CMOS inverter to L. The negative portion of a sine wave drives its output to H. Transitions in the output of the CMOS inverter are sharpened by the Schmitt trigger inverter. Readers can adjust R_1 or R_2 so that the output of Schmitt trigger inverter is a square wave at 50% duty cycle, i.e., half period H and half period L.

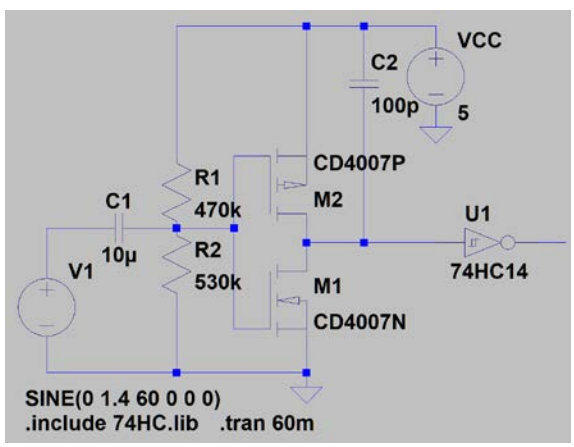


Fig. 6. Synchronized digital clock signal generated from a sinusoidal input. One can use a potentiometer with a resistance of 100 MΩ to replace R_1 and R_2. The middle wiper pin provides a dc bias around 2.5 V to the gate node of the CMOS inverter.

The CD4007 chip can be wired to form other logic gates as shown in the following website: https://wiki.analog.com/university/courses/electronics/electronics-lab-28. For

example, the circuit diagram of a triple input NAND gate is shown in Fig. 7. When will the output become L? (Answer: When all three input signals are H.)

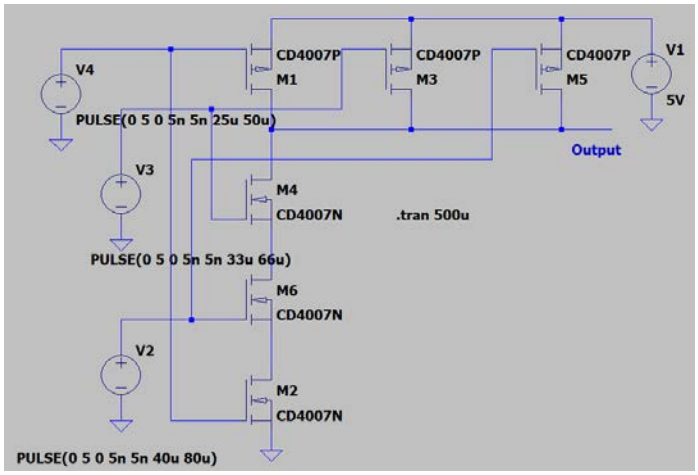


Fig. 7. A CMOS NAND gate with three input nodes, V_2, V_3 and V_4.

In this chapter, we learn the basic characteristics of a CMOS logic inverter. Circuits based on CMOS operate with a low power consumption. With modern design and fabrication techniques, they can reach a switching rate of 5 GHz. In addition to logic ICs, there are also mixed signal ICs based on the CMOS technology. Over 90% of ICs, including camera sensor chips, manufactured nowadays are based on CMOS. They support many applications, including, computers, digital signal processing and communications.

10. Digital Circuits

Combinations of logic gates lead to a great variety of digital circuits, such as arithmetic logic units, digital signal processing units, programming logic control units, etc. Simple functions require few ICs to realize while sophisticated applications may require a field-programmable gate array which is a customizable very-large-scale integration (VLSI) device to implement. In this chapter, we will discuss how to combine logic gates into a data (D) flip-flop and how to use D flip-flops to form counters. We will also discuss how to construct a pseudorandom number generator.

A flip-flop is a bistable device. The output responds to the input by switching between two stable states, H and L. Since it stays in the same state until new input arrives, it serves as a storage device, i.e., a single-bit memory. There are several variations, e.g., RS, D, JK, and T types of flip-flops.

Following ICs are involved: 74HC00, 74HC74 and 74HC86. Their pin configurations are presented in Figs. 1-3.

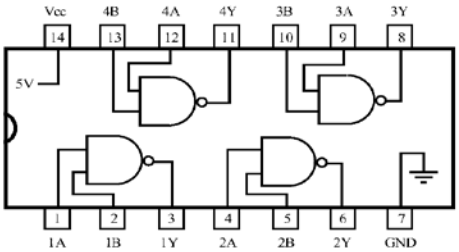
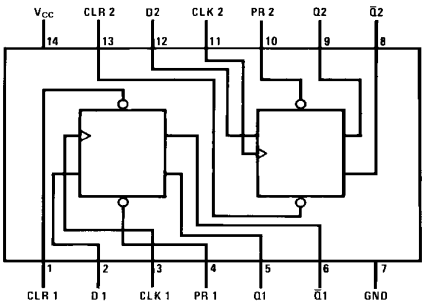


Fig. 1. The pinout configuration of 74HC00 IC. Pin 1 is located at the lower left corner. Pins are arranged in the counterclockwise direction.

Connection Diagram



Function Table

Inputs				Outputs	
PR	CLR	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H (Note 1)	H (Note 1)
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

H = HIGH Logic Level
X = Either LOW or HIGH Logic Level
L = LOW Logic Level
↑ = Positive-going Transition
Q_0 = The output logic level of Q before the indicated input conditions were established.

Note 1: This configuration is nonstable; that is, it will not persist when either the preset and/or clear inputs return to their inactive (HIGH) level.

Fig. 2. The pin configuration and truth table of 74HC74 D flip-flop.

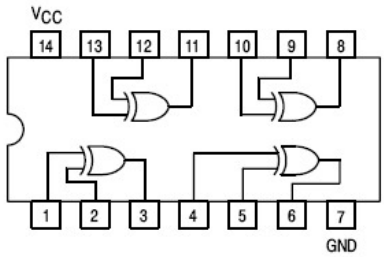


Fig. 3. The 74HC86 XOR.

A D-type flip-flop copies the logic state of the D input to the output under the control of the clock input signal. As shown in Fig. 4, a simplified D flip-flop can be built by using four NAND gates and an inverter. The inverter can be formed by tying two input nodes of a NAND together. It is interesting to note that there are multiple implementations of D flip-flops. Fig. 4 is just one configuration. There are two input nodes, data (D) and clock (CLK), and two conjugate output nodes, Q and $\bar{Q}$.

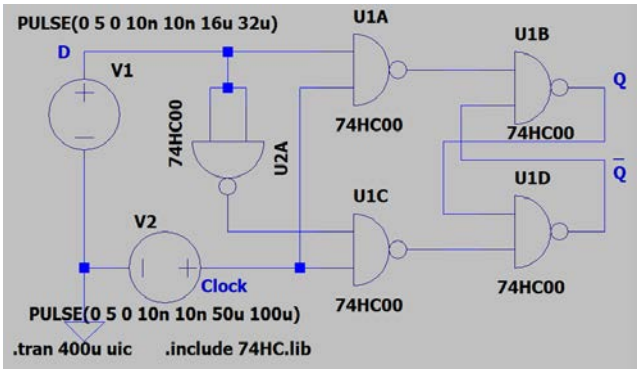


Fig. 4. A D-type flip-flop composed from four NAND gates and one inverter.

There are two digital input signals, a clock signal at 10 kHz and a data signal at 31.25 kHz. Operating the data signal at a higher speed facilitates the interpretation of waveforms. Skipping the initial operating point solution speeds up the transient analysis. Shown in Fig. 5 are waveforms of the two input signals and the output signal. To make it easier to differentiate among waveforms, the clock signal is displayed at full voltage. The data signal is displayed at 90% and the output waveform is displayed at 80%.

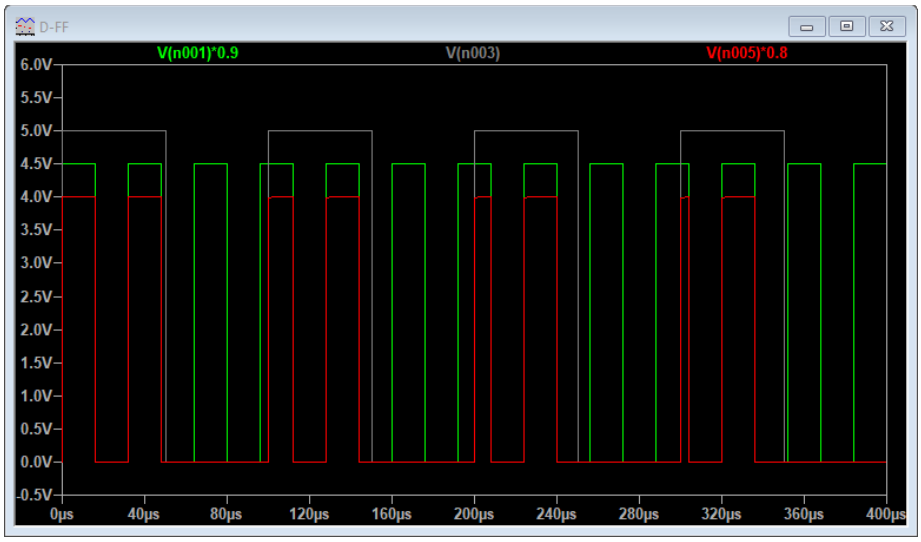


Fig. 5. Waveforms of the D flip-flop circuit. The clock signal is shown in white. The data signal is shown in green. The output waveform is shown in red.

When does the output waveform switch? (Answer: Only when the clock signal is H.) When the clock signal is H, the output follows the data input. When the clock signal is L, the output stays L. Readers can zoom in to examine the switching of input and output waveforms. Is there a delay between the input and output waveforms? (Answer: Yes, around 20-30 nsec.)

Each 74HC74 IC contains two D flip-flops. There are two additional input nodes, preset (PR) and clear (CLR). Its function table is shown in Fig. 2. The output follows the D input signal at the moment when the clock signal makes an upward switching. The output stays unchanged until the next upward switching of the clock signal takes place. This is not the same as how the circuit shown in Fig. 4 operates.

The D flip-flops in 74HC74 can be used to form binary dividers or counters. By cascading N stages, a divide-by-2^N counter is formed. Shown in Fig. 6 is the divide-by-16 counter formed by cascading four stages of D flip-flops Each stage has one clock input and one data input. It has two complementary output nodes, Q and $\bar{Q}$ (not-Q). In addition, there are preset node and clear node to control the state of the D flip-flop.

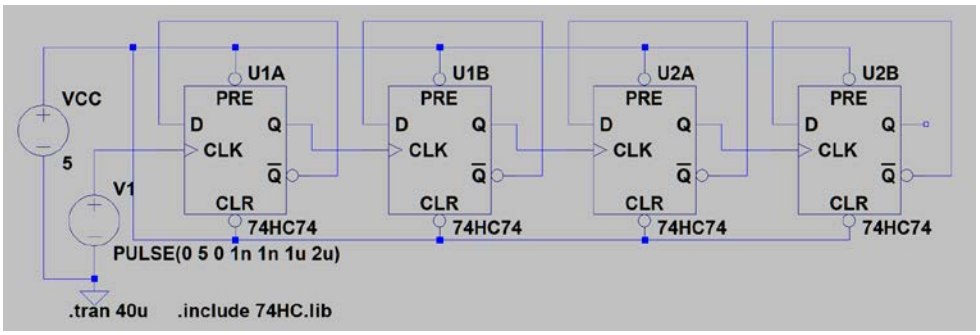


Fig. 6. A divide-by-16 counter based on four D flip-flops in two 74HC74 chips, U1 and U2. Each chip has two flip-flops, A and B. The input is a digital clock signal generated by a waveform generator. The output is at the Q or $\bar{Q}$ node. The diagram shows only logic connections. Power is applied to pin 14 and ground is connected to pin 7 of each chip.

To implement the circuit on a prototype circuit board, connect the 5-V dc power to pin 14 and ground to pin 7 first. Make sure that the power supply and ground connections reach all chips. Any bad connection can prevent the circuit from functioning. The first stage is driven by a square-wave clock signal switching between 0 and 5 V. It is generated by a waveform generator in the pulse mode with following settings: amplitude 2.5 V and offset 2.5 V. The second stage is driven by the output of the first stage, etc. Since there is a propagation delay from stage to stage, there is a delay between transitions of the original clock signal and the output. Such a counter is asynchronous and called a ripple counter.

The following paragraph is prepared for readers who want to build circuits on a prototype circuit board. Tie preset nodes, i.e., pins 4 and 10, of both chips together as one common node. Then connect this common node to logic H, i.e., 5 V. Don't connect pin 4 and pin 10 individually to logic H. You will need this common node later when you build the decade counter. Likewise, do the same for clear nodes, i.e., pin 1 and pin 13. The input clock and the output at the Q or $\bar{Q}$ node can be monitored simultaneously by a dual trace oscilloscope. If you want to visually observe the counter in operation, you can connect an LED in series with a 330-Ω resistor between the $\bar{Q}$ node and ground as an indicator. Set the clock to a very low frequency, e.g., 5 Hz. For oscilloscope observation, run the clock at 1 kHz. Display the input clock signal and the output. Select the output of the divider as the trigger source. If you use the clock signal as trigger, you won't get a stable display. Try it. Can you explain why?

Display the clock signal and the output waveform for each counting stage; from 2 to 16. The output waveform of the divide-by-16 counter is a square wave with 50% time at

H, corresponding to 8 input clock pulses, and 50% at L, also corresponding to 8 input clock pulses. Zoom in the time base of the oscilloscope to a finer scale. Can you determine the delay between the clock signal and the output? Increase the clock frequency if needed. The delay exists in ripple counters. In synchronous counters, all switching events take place in synchronism with the clock signal.

By using logic gates, one can prematurely terminate the counting cycle and form counters for division by a number less than 16, e.g., divide-by-10, divide-by-12, etc. The circuit shown in Fig. 7 is a binary-coded-decimal (BCD) counter. Starting from the least significant bit, which is closest to the clock input, each stage carries a weight of 2^0, 2^1, 2^2, 2^3. The state of the counter is determined by $S_1*2^0+S_2*2^1+S_3*2^2+S_4*2^3$, where S_i is the state of the $\bar{Q}$ node of the i-th stage. The state of each stage can be either zero or one. By monitoring states of S_2 and S_4, the NAND gate can recognize the arrival of 2^1+2^3, i.e., the 10th clock pulse. The output of the NAND gate is connected to the common preset node. It sets all four $\bar{Q}$ nodes to the state of L or 0.

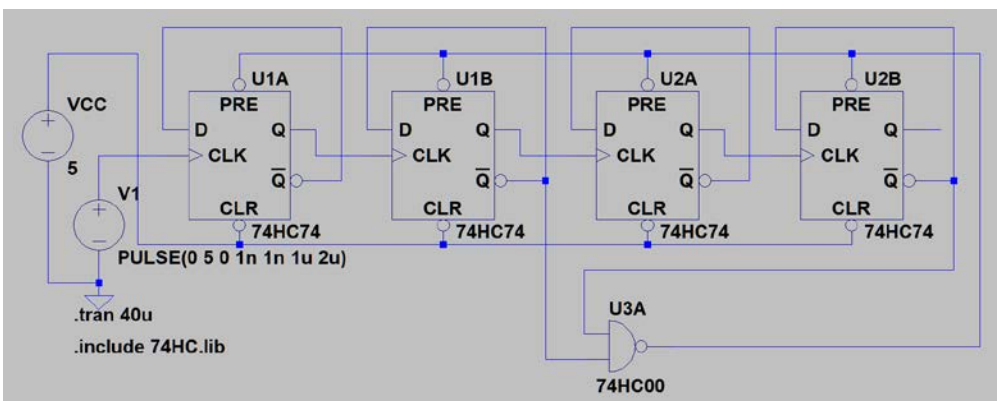


Fig. 7. A divide-by-10, decade counter. The NAND gate monitors the $\bar{Q}$ nodes of the second (2^1) stage and the fourth (2^3) stage. All preset nodes are connected to the output of the NAND gate. The output is at the Q or $\bar{Q}$ node of the last counter stage.

During each period of the decade counter, the waveform at the Q node spends 80% time on H and 20% on L. Such a waveform has a duty cycle, i.e., percentage of time in the H state, of 80%. Of course, if you monitor the output at the conjugate node, $\bar{Q}$, the duty cycle is 20%. Instead of using the circuit diagram shown in Fig. 7, one can build another decade counter by cascading a divide-by-5 counter and a binary, i.e., divide-by-2, counter. To realize the divide-by-5 counter, you need to monitor 2^0 and 2^2 stages. Connect the $\bar{Q}$ node of both stages to the input of the NAND gate. The output of the NAND gate is

connected to the preset nodes of the front three stages. The preset node of the last binary divider and all clear notes are connected to H, i.e., the power supply. With a binary counter as the last stage, the duty cycle will be 50%. Can you come up with the circuit diagram of a divide-by-12 counter? Can you also design a divide-by-13 counter? (Hint: you need a triple NAND gate which can be composed by using two NAND gates and one inverter.)

In addition to counters, one can also form a shift register by cascading D flip-flops. Furthermore, by adding an XOR gate, one can form a pseudorandom number generator. A pseudorandom sequence consists of random digital pulses. It has a finite length. After one complete cycle, the pattern repeats itself. The sequence generated depends on how the XOR gate is configured. The longest sequence is 2^N-1, where N is the number of flip-flops. For N=4, this is accomplished by using the 3rd and the 4th D flip-flops to drive the XOR gate as shown in Fig. 8. The output is located at the $\bar{Q}$ node of the last D flip-flop.

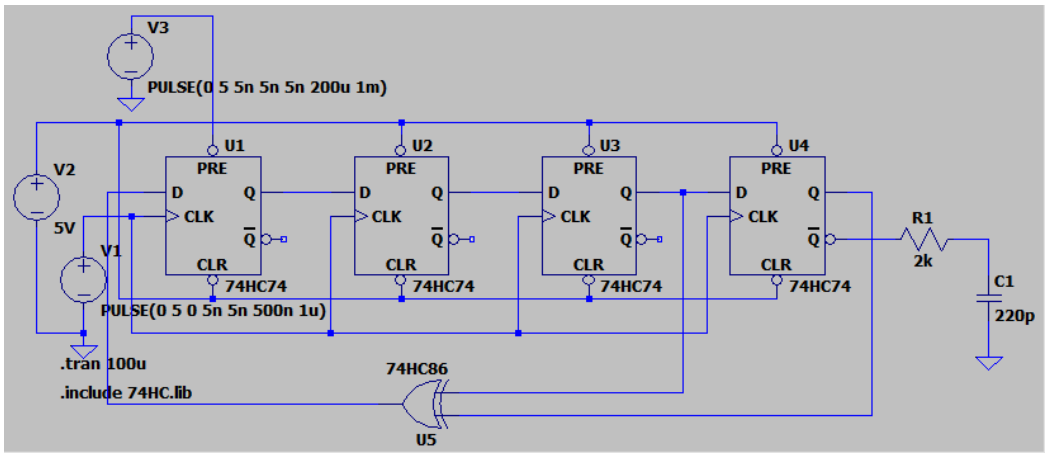


Fig. 8. A pseudorandom number generator circuit. In this configuration, the control signal is derived from the third and the fourth shift registers. Logic H is provided by the +5 V power supply. The voltage source, V_1, is a clock signal. The voltage source, V_3, provides a L to H transition. It initiates the pseudorandom number generator. The output is located at the $\bar{Q}$ node of the last D flip-flop. In real circuit implementation, V_3 is replaced by a jumper wire which can be manually toggled to and from the ground. The low-pass filter emulates the bandwidth limitation.

There are applications for the pseudorandom number generator in digital communications systems. One specific application is the testing of system performance. The output of the pseudorandom number generator closely matches the signal at the transmitter end of a digital communications system. There are random pulses of H and L

with varying duration. After repetitive sampling, the accumulated waveforms merge together to become an eye diagram. LTspice has the feature of displaying the eye diagram. Display the waveform. Right click the horizontal axis. Select and enable the eye diagram. Enter the frequency of the clock signal as the baud rate. Enter the number of eyes to show. Zoom in to fit. The eye diagram is shown in Fig. 9.

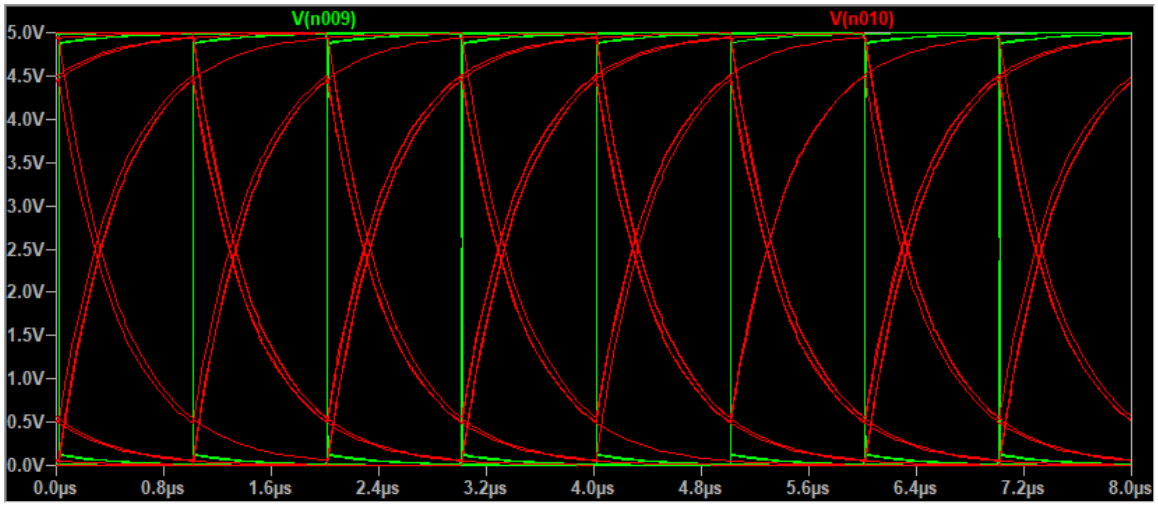


Fig. 9. The eye diagram displayed by LTspice. The green waveform is the output of the pseudorandom number generator. The red waveform is the output of the low-pass filter. The low-pass filter simulates the bandwidth limitation of a digital communications system.

In each timing interval, the signal can be H or L. An upward transition and a downward transition exist in the wings. At the transmitter end, the clarity between H and L is very high. The eye is widely open. At the receiving end, due to the dispersion, bandwidth limitation and timing jitter, the eye becomes partially closed. The low-pass filter in the circuit diagram shown in Fig. 8 emulates the bandwidth limitation. Its output provides an example of the waveform at the receiver. Indeed, the “eye” of the red waveform is partially closed. When noise or timing jitter is present, a partially close eye leads to error bits. The performance of the digital communications system is linked to how wide the eye opening is. Readers can increase the clock to 4 MHz to see an example of closed eye diagram.

In this chapter, we learn how to combine logic gates into flip-flop and counters. We also learn how to generate a pseudorandom digital signal. The pseudorandom number generator finds applicaitons in communications systems.

11. Analog-to-Digital Conversion

Computers and micro-controllers operate with digital signals. On the other hand, audio, video, sensors and control often involve analog signals. The analog-to-digital (A/D) and digital-to-analog (D/A) converters provide the necessary interface. During the conversion process, a continuously changing analog waveform is periodically sampled. Result are quantized into a finite number of discrete levels. Two parameters determine the accuracy of the conversion process. The first is the sampling rate which is closely related to the bandwidth of the signal. A broadband signal must be sampled at a high sampling rate. Let's consider a sine wave. The A/D process must at least pick up two points, i.e., the positive and the negative extremes, in a sinusoidal cycle. The sampling needs to run at the Nyquist rate, i.e., twice the frequency. Under sampling leads to aliasing. The second consideration is how accurate the sampled results need to be. Quantization turns the sampled analog signal into a finite number of discrete levels using 1 bit, 8 bits, 12 bits, 16 bits, etc. Obviously, a 16-bit system has a much finer resolution than an 8-bit system. The sampling rate and the number of bits determine the accuracy.

There are different A/D and D/A converters. We will focus only on the sigma-delta modulator. It uses the pulse-density modulation to convert an analog signal into digital pulses. It is a single-bit A/D converter running at a high sampling rate. The circuit diagram is shown in Fig. 1. There are two input signals. The digital clock signal, V_1, controls the sampling rate. The signal source, V_2, is the analog input with an amplitude of 2.5 V and a dc offset of 2 V. The digital output signal appears at the $\bar{Q}$ node of the D flip-flop.

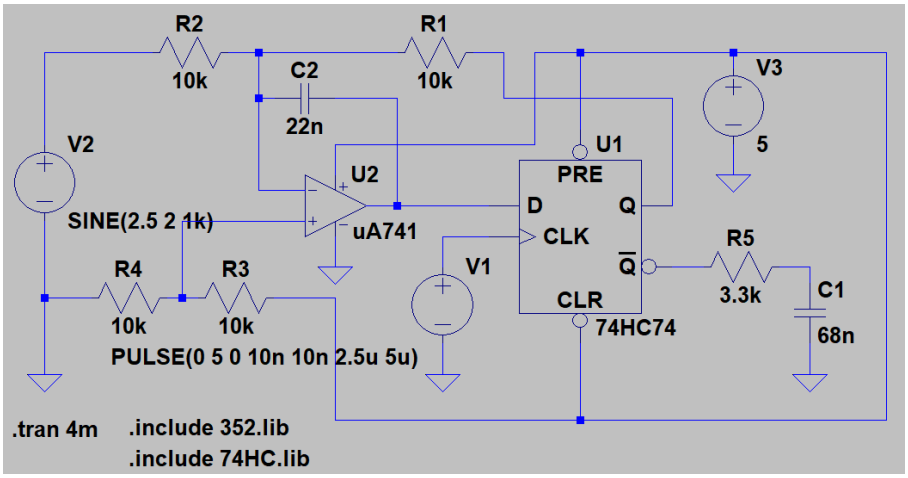


Fig. 1. The circuit diagram of a sigma-delta modulator.

The circuit in Fig. 1 process signals in hardware. Using the capacitor, C_2, the operational amplifier integrates both the analog input signal via R_2 and the conjugate or negative of the digital output via R_1. The D flip-flop serves as a single-bit quantizer. The circuit runs with a single +5 V power supply. Two resistors, R_3 and R_4, form a voltage divider providing the +2.5 V reference to the non-inverting input node of the operational amplifier. After running the transient simulation, one can observe the input and output waveforms as shown in Fig. 2. The input sine wave is converted into digital pulses. When the sine wave is near its positive extreme, the digital output is mostly H. When the sine wave is near its negative extreme, the digital output is mostly L. Readers can also display the waveform at the D input node of the flip-flop to see how the single-bit quantizer operates.

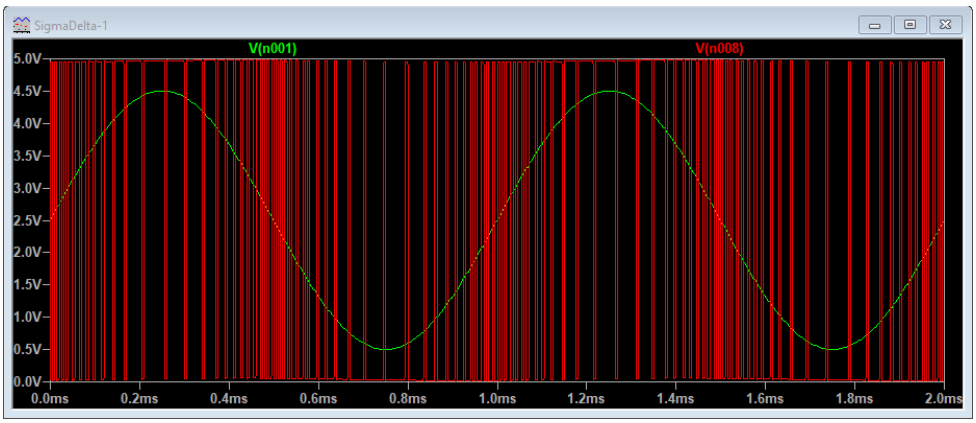


Fig. 2. The sine wave input and the digital output waveforms of the sigma-delta modulator.

The digital output of the sigma-delta modulator can be converted back to an analog signal by using a low-pass filter consisting of R_5 and C_1. It integrates the digital pulses to recover a proportional but delayed copy of the sinusoidal signal. Display the input sine wave and the output of the low-pass filter as shown in Fig. 3. The delay and the amplitude of the output are related to the frequency of the signal and -3dB frequency of the low-pass filter. As shown in Fi. 3, there is a difference between the original analog signal and the output of the low-pass filter. The difference indicates that digitization has a finite accuracy. A lower clock rate or sampling frequency will result in a lower digitization accuracy. Reduce the frequency of the clock signal gradually from 200 kHz, 100 kHz, 50 kHz, to 25 kHz. Monitor the output of the low-pass integrator. The zig-zag increases as the clock frequency is reduced. If you need to convert an audio signal up to 20 kHz, what will you do in setting the frequency of the clock?

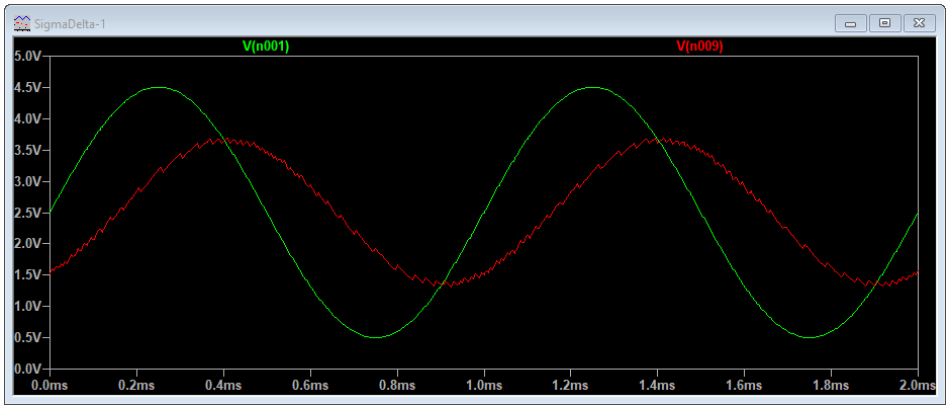


Fig. 3. The sine wave input and the recovered analog signal after the low-pass filter. Both the amplitude and the degree of zigzagging depend on the $R{\cdot}C$ time constant of the low-pass filter. With the same low-pass filter, the amount of zigzagging increases as the clock frequency, i.e., sampling rate, is reduced.

In this chapter, we combine the previously studied integrator and D flip-flop to form a sigma-delta modulator. The sigma-delta modulator is a single-bit A/D converter running at a frequency much higher than the Nyquist rate. This is called oversampling. The circuit provides an opportunity to study how the sampling rate affects the accuracy of A/D. If you are interested in studying the D/A conversion, you can search and read about the R-2R converter. There are dedicated A/D and D/A ICs. Micro-controllers have A/D and D/A capability built in. Digital signal processing chips can also provide the interface between analog signals and digital systems.

There are tutorials online. To learn more about the sigma-delta modulator, please browse: https://training.ti.com/delta-sigma-adcs-overview. For an introduction to R-2R A/D, please browse: https://www.tek.com/blog/tutorial-digital-analog-conversion-r-2r-dac.

12. Differential Amplifier

The differential amplifier is important. The input stage of most operational amplifiers is a differential amplifier. Differential amplifiers can provide a large voltage gain. They can also suppress noise present in the surrounding environment. They can perform operations, such as multiplication and modulation. In this chapter, we learn the operational principle, build the circuit, and characterize the performance of a differential amplifier.

A typical differential amplifier circuit is shown in Fig. 1. Two transistors, Q_1 and Q_2, form a differential amplifier. Two base nodes are input ports. Two collector nodes are output ports. When voltages are applied to the two input ports, the differential amplifier provides a large gain to the difference of input voltages. It provides no gain to the common signal present on both input nodes. Transistors, Q_3 and Q_4, form a constant current source. A constant current source dynamically adjusts its output voltage according to the condition of the load. Over a wide range of load resistance, it can maintain a constant current. The effective output impedance of a constant current source is very large.

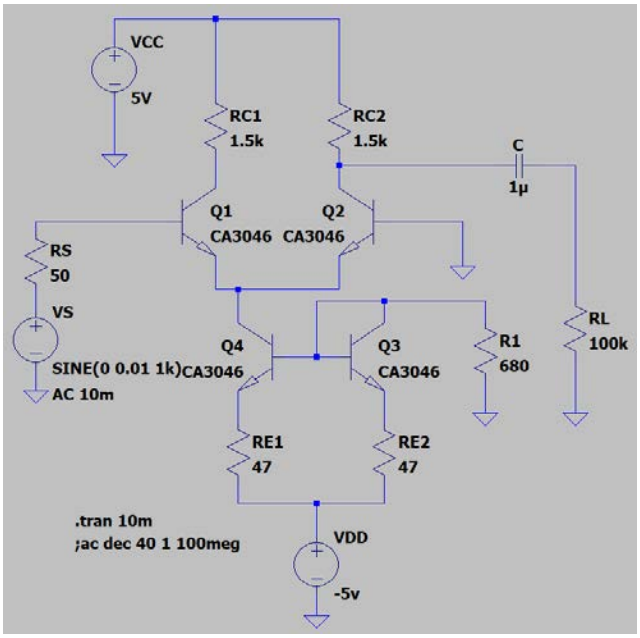


Fig. 1. The schematic diagram of a differential amplifier circuit. You can use a CA3046 transistor array. You can also use 2N3904 or other transistors. The pair, Q_1 and Q_2, should be of the same model number. So are Q_3 and Q_4.

The output can be taken between the collector of either transistor and the ground. It can also be taken between two collectors. Since the polarity is opposite between two collectors, there is a push-pull effect. To probe the output with an oscilloscope which has a ground connection, the output can only be monitored between one collector node and the ground. If the collector of Q_2 is the output port, the non-inverting input port is the base of Q_1. The inverting input port is the base of Q_2.

A differential amplifier can be analyzed for two different operational modes separately. The differential mode is realized by applying voltages of opposite polarity to two input ports. For example, apply V_s to the base of Q_1 and $-V_S$ to the base of Q_2, i.e., $V_1 = -V_2 = V_s$. The voltage, V_1, represents the voltage applied to the base node of Q_1 and V_2 represents the voltage applied to the base node of Q_2. The increase in emitter current of Q_1 is compensated by a corresponding decrease in the emitter current of Q_2. Therefore, the emitter voltage, V_E, is unchanged. For an ac signal, the emitter node is virtually grounded in the differential mode. Each transistor becomes a common-emitter amplifier. The voltage gain of an individual transistor is

$$A^{diff} = -g_m R_C. \tag{1}$$

Since there is no coupling capacitor, the differential amplifier works all the way to dc. There is no low-frequency cutoff. To characterize the gain at dc, the output voltage is measured as the deviation from the Q-point voltage; not the dc voltage directly measured as is. In other words, you have to use the Q-point collector voltage with zero input, i.e., both base input nodes connected to the ground, as the baseline. After changing the base voltage, measure the new collector voltage. Subtract the baseline voltage to derive the dc output voltage. In the differential mode, the amplifier has characteristics, i.e., input impedance and output impedance, identical to those of a common-emitter amplifier.

The common mode is realized by applying the same voltage to both input ports. In the common mode, both transistors try to increase the emitter current which, in turn, increases V_E. This cancels out the increase in the input voltage. To analyze the common-mode gain, one can split the circuit symmetrically. Assuming that the impedance of the constant current source is r_o, each BJT amplifier now has a large emitter resistance, $2 \cdot r_o$. The voltage gain of each transistor is

$$A^{comm} \cong -g_m R_C / [1 + g_m (2r_o)]. \tag{2}$$

Since r_0 for a constant current source is very large, the common-mode gain is less than unity. In other words, it is not a "gain" but a loss or an attenuation factor.

To characterize the differential amplifier via measurements, the input signal, V_{in}, is only applied to one input port while the other input port is grounded. In this case, the input signal can be considered as a combination of differential and common modes.

$$V_o = -A_v^{diff} \cdot V_{in}/2 + A_v^{comm} \cdot V_{in}/2. \tag{3}$$

Since the common-mode gain is small, the second term can be neglected. The differential gain is $2 \cdot V_o/V_{in}$.

In order to bias transistors in the active region when both input ports are grounded, a dual voltage power supply is needed. If transistors are poorly matched, the performance of the circuit may deteriorate, e.g., a substantial increase in the common-mode gain. A simple way to check whether transistors are reasonably well matched is to measure the Q-point voltages at collector nodes of Q_1 and Q_2. The Q-point voltages should be nearly equal. If they are very different, replace with a pair of matched transistors. One can simulate the mismatch by placing transistors of different models in the circuit.

To design a differential amplifier schematically shown in Fig. 1, go through the following procedures:

1. Pick voltages for the dual power supply, e.g., V_{CC}=5 V and V_{DD}=-5 V. Again, the voltage is flexible but should not be excessive.
2. Pick R_{C1}=R_{C2} according to the desired output impedance, e.g., 1 kΩ.
3. The Q-point condition is determined by grounding both input ports. The voltage drop from V_{CC} to the emitter node of Q_2 is V_{CC}+0.7 V, i.e., 5.7 V, assuming that the power supply is at 5 V. To get the maximum output voltage swing without clipping, the collector of Q_2 should be at approximately (5-5.7/2) V, i.e., 2.15 V. The collector current is, therefore, (5-2.15)V/R_{C2}, i.e., 2.85 mA. The total current flowing through Q_3 is twice the current flowing through Q_2, i.e., 5.7 mA.
4. For R_{E1} and R_{E2}, 47-Ω resistors are used at emitter nodes of Q_3 and Q_4 for stabilization.
5. The current of Q_4 should be the same as the current of Q_3, i.e., 5.7 mA.
6. Consider the loop from the ground through R_1, V_{BE}, to V_{DD}. The resistance, R_1, can be determined as (|V_{DD}|-0.7 V)/5.7 mA-47 Ω. You only need to adjust R_1 to optimize the bias condition.

Follow design procedures to build the differential amplifier schematically shown in Fig. 1. Use V_{CC}=5 to 10 V and V_{DD}=-5 to -10 V. Ground both input ports. Record dc Q-

point voltages. Make sure that transistors are all biased in the active region, i.e., V_{BE}≈0.7 V. The dc Q-point can be adjusted by changing the value of R_1 in Fig. 1.

Use a 1-kHz, 20-30 mV peak-to-peak, sinusoidal signal as V_1. Keep V_2 grounded. Use the oscilloscope to monitor the output voltage between the collector of Q_2 and the ground. Determine the ac voltage gain. Measure the gain again by taking the output between the collector of Q_1 and the ground. Compare voltage gains measured at collectors of Q_1 and Q_2. They should be nearly the same except that the phase is opposite. Ground V_1 and apply a small voltage to V_2. Measure the voltage gain again. It is important to notice the phase of the output waveform.

Obtain the frequency response curve, i.e., the Bode plot. Determine the -3 dB point at high frequency. Increase the amplitude of the input signal until the output waveform becomes clipped. Adjust R_1 to see whether waveform clipping can be eliminated. Record the maximum voltage swing without clipping. In linear amplifiers, adjustment or optimization of the bias condition is the most critical task in design and operation. Apply the same voltage to both input ports simultaneously. Measure the common-mode voltage gain. Since the common-mode “gain” can actually be loss or attenuation, a large input signal is needed.

In integrated circuits, semiconductor devices are preferred to resistors. The collector resistor in a differential amplifier can be replaced by an active load, i.e., a transistor in the constant current source configuration as shown in Fig. 2. Since the effective resistance of a constant current source is high, the gain is high. Such a circuit forms the front end of an operational amplifier.

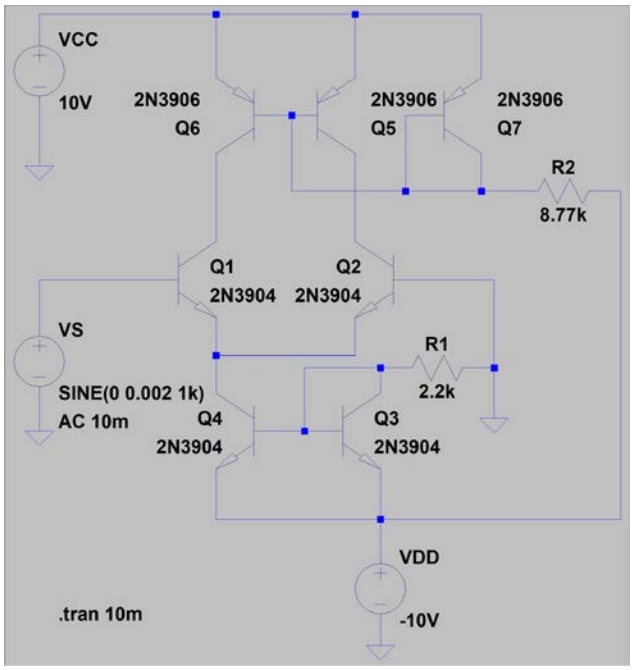


Fig. 2. The circuit diagram of a differential amplifier with one active load at the collector node of each transistor.

In this chapter, we study the differential amplifier circuit. In the differential mode, it provides a voltage gain like a common-emitter amplifier. In the common mode, it provides a small output signal. The differential amplifier is used in operational amplifiers. It is also used to generate modulated signals in communications systems.

13. Multi-Stage Amplifier Project

The performance of a single stage amplifier is limited. By cascading several amplifier stages, one can build a circuit meeting multiple design goals. The operational amplifier is an example. It clearly demonstrates the benefit of multi-stage amplifiers. In a multi-stage, amplifier, each amplifier stage can be designed for meeting a specific performance requirement. For example, the first stage can be designed to meet the input impedance requirement. The middle stage can be used to boost up the gain. The last stage can be designed to meet the output impedance requirement. The main concern of a multi-stage amplifier design is the loading effect. The second stage becomes the load of the first stage. The input impedance of the second stage must be taken into consideration while designing the first stage. Furthermore, the dc quiescent conditions of two stages may not match. The purpose of this chapter is to learn how to design, construct, and characterize a multi-stage amplifier circuit.

Decisions to make in designing a multi-stage amplifier include the selection of semiconductor components and amplifier configuration. Knowledge of semiconductor components and basic amplifier circuits can help in designing multi-stage amplifiers. For example, an FET amplifier can provide a very large input impedance. A common-collector amplifier can provide a low output impedance. A common-emitter stage can provide a large voltage gain. The main complication in designing a multi-stage amplifier is the loading effect. The input impedance of the following stage must be included in calculating the gain of the stage in the front. It is, therefore, logical to design a multi-stage amplifier starting from the last stage. You can use its input impedance as the load when you design the amplifier in front of it. In general, you want to keep the output impedance of the front stage lower than the input impedance of the next stage. Since an FET has a high input impedance, the effect of loading can be greatly reduced if the circuit is built with FETs. However, since the voltage gain of an FET amplifier is small, more stages may be required to reach the overall voltage gain desired. If only ac gain is needed, you can use coupling capacitors between stages. The dc bias conditions can be determined separately for each stage independent of the subsequent stage.

The overall gain of a multi-stage amplifier is given by the product of amplification factors of individual stages. The frequency responses of individual stages can affect the overall frequency response of a multi-stage amplifier. Usually, the stage with the narrowest frequency response determines the overall bandwidth. The low-frequency response can be

limited by the bypass capacitor at the emitter or source node. Electrolytic capacitors with larger capacitances can be used to extend the low-frequency response. As you increase the capacitance of the bypass capacitor, the time that it takes for the amplifier to reach the steady state also increases. You will notice that the gain drifts when the power supply is just turned on. Occasionally, the coupling capacitors between stages limit the low-frequency response. The bottleneck can be relieved by simply increasing the capacitance of the limiting coupling capacitor. The high-frequency response is limited primarily by the junction capacitance of semiconductor components. The common-base configuration provides a better high-frequency response. Lowering the gain of a common-emitter amplifier can also extend the high-frequency response.

To practice multi-stage amplifier design, readers are to design a multi-stage amplifier to meet the following specifications:

- An input impedance ≥ 200 kΩ
- An output impedance ≤ 200 Ω
- A voltage gain ≥ 300 (150 if you use +5 V power supply)
- A low-frequency -3 dB point ≤ 50 Hz
- A high-frequency -3 dB point ≥ 15 kHz
- An output voltage swing ≥ 4 V peak-to-peak without distortion (2 V for +5 V supply)

Select components and amplifier configurations. For example, pick an FET amplifier as the first stage to meet the input impedance requirement. Pick a BJT amplifier in the common-collector configuration as the last stage to meet the output impedance requirement. Pick one or even two BJT amplifiers in the common-emitter configuration to meet the gain requirement. Start composing the circuit diagram by drawing the last stage first. Since a common-collector amplifier provides no voltage gain, use a signal source with an amplitude of 2 V as the input to test the last stage. Use ac coupling, i.e., insert a coupling capacitor between the signal source and the base node. Adjust the bias condition so that the output waveform is not clipped. Attach a load resistor through a coupling capacitor. Determine the output impedance. The output impedance of the common-collector amplifier can be very low, i.e., in the 10 Ω range. Reduce the output signal to <0.4 V peak-to-peak to prevent waveform clipping. Since the load resistance is low, you need a large coupling capacitor, e.g., 220 μF. You can also perform the measurement at a higher frequency, e.g., 10 kHz, instead of 1 kHz. You only need to see a measurable reduction in the output voltage. You can then use the voltage divider formula, $V=V_{NoLoad}\cdot R_L/(Z_o+R_L)$, to derive the

output impedance, Z_o. The output impedance can be reduced by reducing the resistance of the emitter resistor. After optimizing the last stage, compose the middle stage. Attach the last stage through a coupling capacitor to the middle stage. The last stage becomes the load of the middle stage. You need a signal source with a small amplitude as the input of the middle stage. Optimize the bias condition. Determine the voltage gain. Since the first stage also provides a gain, the gain of the middle stage only needs to be around 150. Finally, compose the first stage. Its output is connected to the second stage through a coupling capacitor. The second stage can substantially load down the gain of the first stage. The signal source with a very small amplitude is connected to the input. Adjust the bias condition.

Find dc operating conditions and the ac performance by running the circuit simulation program. Verify that all design goals are met. If not, redesign the circuit. By now, you should know how to improve the design. For example, if the low-frequency cutoff is too high, which capacitor or capacitors should be increased? If the voltage gain is not sufficient, which resistor should be changed to get extra gain? If the waveform clipping occurs, which bias resistor should be adjusted? Since there are quite a few components, you will be frustrated if you try to improve the circuit by guessing randomly.

Demonstrate that the circuit meets all design specifications. Provide data as verification of the circuit operation by going through the following design checklist:

- A_V at 1 kHz
- Peak-to-peak output voltage without distortion
- Low-frequency -3dB point
- High-frequency -3dB point
- Input resistance at 1 kHz
- Output impedance at 1 kHz

The following information is provided specifically for readers who would like to physically implement the circuit on a prototype circuit board. The gain is high. The number of devices is substantially larger than that of a single-stage amplifier. The stray capacitance or inductance can cause self-oscillation. Build the circuit neatly, i.e., with short jumper wires to suppress self-oscillation. Place a 1-μF capacitor between the power supply bus and the ground on the prototype board. If oscillation still persists, a small, e.g., 10 to 100-pF, capacitor can be added between the collector and the base of BJT to suppress the high-frequency gain, hence, to eliminate the high-frequency self-oscillation.

If the circuit constructed doesn't work initially, you have to perform trouble shooting. You should measure dc voltages first. Measure the power supply bus on the prototype board, the collector of each BJT and the drain of each FET. Make sure that all devices are properly biased. Then, monitor the ac waveforms at different locations using the oscilloscope probe. Are all components properly connected? Are all electrolytic capacitors connected with the proper polarity? Is there any potentiometer adjusted to its extreme? If you suspect any semiconductor device, replace it. The low-frequency response can be improved by increasing values of bypass capacitors and coupling capacitors. Do you have a large enough $R \cdot C$ value? The high-frequency response can be improved by reducing the gain. If the loading is severely limiting the gain of the front stage, you may consider using a high impedance device, e.g., FET, or adding a common-collector buffer stage, which has a high input impedance and low output impedance.

14. Negative Feedback and Push-Pull Amplifier

In circuits with feedback, a portion of the output is connected to the input. Feedback plays an important role in electronics. There are two feedback conditions. If the signal derived from the output is in phase with the input signal, the feedback is positive. If the phase of the feedback signal is opposite to that of the input signal, a negative feedback is realized. Positive feedback leads to oscillators. Negative feedback can improve the circuit performance.

Large signal circuits, notably power amplifiers, are subject to distortions. However, high linearity is crucial for many applications. For example, audio amplifiers rated at 100 W and above are very common. An audio amplifier must be linear to reproduce music with high fidelity. Certain telecommunication equipment must be very linear. Otherwise, there will be crosstalk and interference. Amplifiers built with discrete components are not ideal. As the signal level increases, the output waveforms of BJT and FET amplifiers become distorted. Serious distortion like waveform clipping can be avoided by adjusting the bias. However, large sinusoidal waveforms are always somewhat rounded at the top because the transconductance of a transistor is current dependent. In other words, semiconductor devices are not intrinsically linear. The goal of this chapter is to explore how to use feedback to improve the performance of amplifiers. We will build a BJT common-emitter amplifier with negative feedback and a class B, push-pull amplifier. With a proper feedback amplifiers can offer lower distortion and better frequency response.

The resistor between the emitter and the ground in the common-emitter BJT amplifier is an example of negative feedback. Because of the presence of a bypass capacitor, the feedback only affects the dc. It is used to stabilize the circuit against device and temperature variations. To extend the negative feedback to ac, we can remove the bypass capacitor. The circuit diagram of a BJT common-emitter amplifier with negative feedback is shown in Fig. 1. For readers to easily compare its performance to a BJT amplifier without negative feedback, the bypass capacitor is shown but not connected in the circuit diagram. The output ac signal at the collector is derived from $i_C \cdot R_C$. The ac collector current also flows through the emitter. There is a voltage drop developed across R_E. The feedback voltage affects the emitter voltage, hence, the base current. When a positive input signal is applied to the base, the negative feedback resistor increases the voltage at the emitter. This feedback voltage partially compensates the input signal at the base. The partial compensation of the input signal by sampling the output forms the basis of negative

feedback. There larger the R_E, the stronger is the negative feedback. Of course, because of signal cancellation, the negative feedback decreases the voltage gain. The reduction can be substantial. However, higher linearity and wider bandwidth can be realized. If needed, the gain can always be boosted by adding another amplifier.

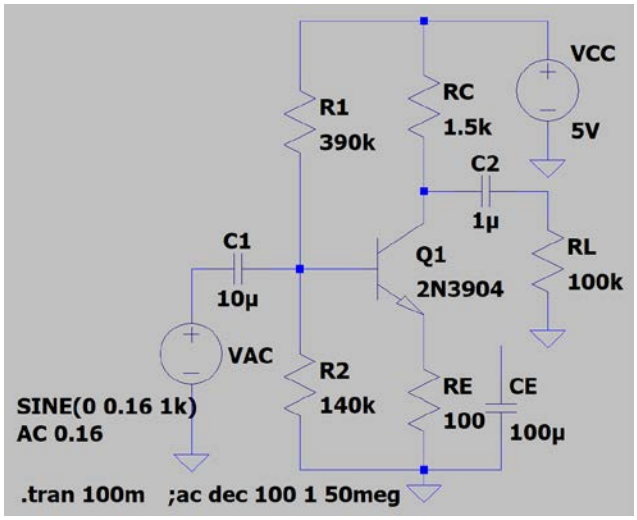


Fig. 1. The schematic diagram of a common-emitter amplifier with negative feedback.

In addition to components explicitly drawn in the circuit diagram, there are junction capacitances in the transistor, in particular, C_μ. It is located between the base and the collector. In the common-emitter configuration, the base is the input node. The collector is the output node. The junction capacitance, C_μ, causes a negative feedback because the output is at 180^0 off. Because of the gain of the amplifier, the effect of this junction capacitance on the frequency response is greatly amplified via the Miller effect. It can limit the high-frequency response. You can find details of the Miller effect in a textbook or online.

Run the simulation on the circuit shown in Fig. 1. Obtain the waveform, FFT and the Bode plot. For comparison, connect the bypass capacitor back to the emitter to form a BJT amplifier without negative feedback. Reduce the amplitude of the input signal to 25 mV so that the output voltage remains approximately the same. Run the simulation. Obtain the waveform, FFT and the Bode plot. Compare waveforms. Which waveform has less rounding at the top? Compare the FFT spectra. Which one has a lower second harmonic distortion relative to the peak at the fundamental frequency? Compare two Bode plots. Which circuit has a broader frequency response? Which circuit has a higher voltage gain?

An operational amplifier has two input nodes. To realize an amplifier, a portion of the output is connected via a feedback resistor to the inverting input node. A class B, push-pull amplifier is shown in Fig. 2. The 2N3904 npn and 2N3906 pnp BJTs form a complementary pair. They are in the emitter-follower configuration to provide a low output impedance. During the positive half cycle of the input at the base node, the npn BJT conducts. During the negative half cycle of the input, the pnp BJT conducts. There is no standby dc bias current going through both transistors at the same time. Therefore, the power internally dissipated by transistors can be reduced. The class B amplifier offers a better efficiency. Many audio systems use the class B amplifier as the output stage. Before the input reaches the voltage needed to forwardly bias the base-emitter junction, i.e., V_{BE}=0.7 V, there is no output at the emitter. The output waveform becomes distorted when the input signal is crossing over the zero voltage. Depending on how the circuit is configured, the class B push-pull amplifier can suffer from the cross-over distortion. One way to eliminate the cross-over distortion is to bring the output back to the inverting input of the driving operational amplifier. In the cross-over region between 0 and 0.7 V, the operational amplifier provides a fast rising signal, limited only by the slew rate, to turn transistors on. You can visualize the circuit in operation by monitoring the input signal, the output of the operational amplifier and the output of the class B amplifier.

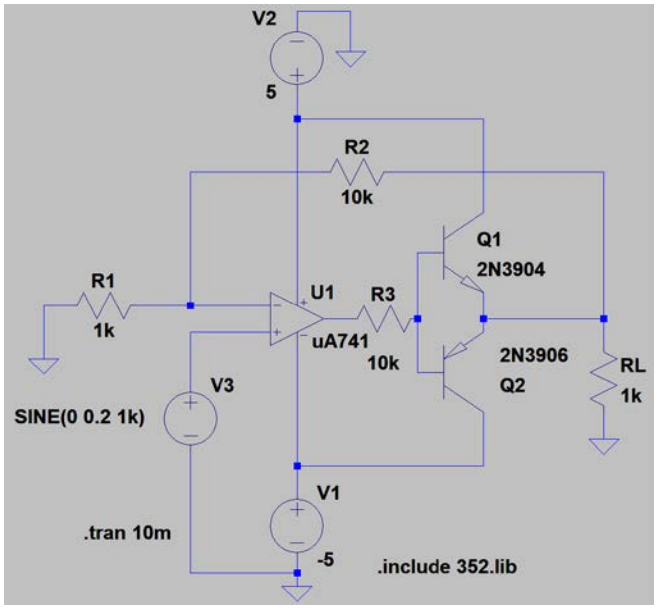


Fig. 2. The schematic diagram of a class B amplifier. The power supply voltage is flexible. It can be from ±5 V to ±15 V.

Drive the operational amplifier shown in Fig. 2 to obtain a 4-V peak-to-peak output voltage at 1 kHz. Record waveforms. Revise the circuit. Connect R_2, the feedback resistor, to the output node of operational amplifier instead of the emitter node of BJTs. Obtain waveforms again. Can you see the cross-over distortion?

In summary, negative feedback involves bringing a portion of the output back to the input with a phase shift of 180^0. Negative feedback leads to a lower gain. However, circuits with negative feedback offer better performances both in linearity and the frequency response. The reduction in gain can be compensated by adding another amplifier. The class B amplifier offers improved efficiency. It requires a properly connected signal to eliminate the cross-over distortion.

15. Positive Feedback and Oscillators

Oscillators are for signal generation. They are indispensable. In this chapter, we learn the basic operational principle of oscillators. We also study circuits to generate sinusoidal and square-wave signals.

Oscillation starts from the amplification of noise. When there is an in-phase, positive feedback from the output of an amplifier back to its input, the amplitude grows. Eventually, the output stops growing because of the gain saturation or waveform clipping. In the steady state, the loop gain from the input to output then back to the input through feedback is exactly unity. The oscillation frequency is determined by the condition that the feedback from output back to the input, including the propagation delay, is in phase, i.e., zero or a multiple of 360^0.

There are two types of oscillators, namely, sine wave and square wave. An oscillator starts with a loop gain higher than one initially to build up its output. Eventually it reaches a stable output when the gain saturates. If the gain saturates because the output is limited by the power supply voltage, the waveform is clipped and looks like a square wave. To get a sinusoidal output, an oscillator must self-regulate its gain. Shown in Fig. 1 is the circuit diagram of a Wien bridge oscillator. It is included in the LTspice distribution. The Wien bridge oscillator generates a sinusoidal wave. The operational amplifier is configured as a non-inverting amplifier. The phase, hence, the oscillation frequency, is determined by $R{\cdot}C$ in the positive feedback loop. Since the feedback loop in Fig. 1 provides a peak feedback factor of 1/3 at the oscillation frequency, the operational amplifier needs to provide a gain of 3 to reach a loop gain of unity. The gain is determined by R_1, R_2 and the equivalent resistance of the JFET, Q_1. The signal diode, D_1, is a rectifying diode. The capacitor, C_3, filters the ripple. Together, they provide a negative dc voltage to bias the gate of Q_1. When the output voltage of the oscillator is low, the gate bias voltage of Q_1 is close to zero. Q_1 conducts and its resistance is low, hence, the gain of the amplifier is high. When the output voltage is high, the gate voltage becomes more negative leading to a reduced current and a higher resistance for Q_1. The gain of the amplifier decreases. Run the simulation. Display the output waveform. View FFT to determine the oscillation frequency. Increase the capacitance of both capacitors in the feedback loop by a factor two. Find the frequency. Is the frequency inversely proportional to the capacitance? Only when the total resistance of R_2 and Q_1 is exactly 500 Ω, i.e., the gain of the non-inverting amplifier is exactly 3, the oscillator can generate a sine wave. Replace the self-regulating Q_1 with a fixed resistor.

Start with 100 Ω. The circuit generates a clipped waveform. Change to 330 Ω. The circuit no longer oscillates. Because the bandwidth of the operational amplifier is limited, the Wien bridge oscillator only works in the kHz range.

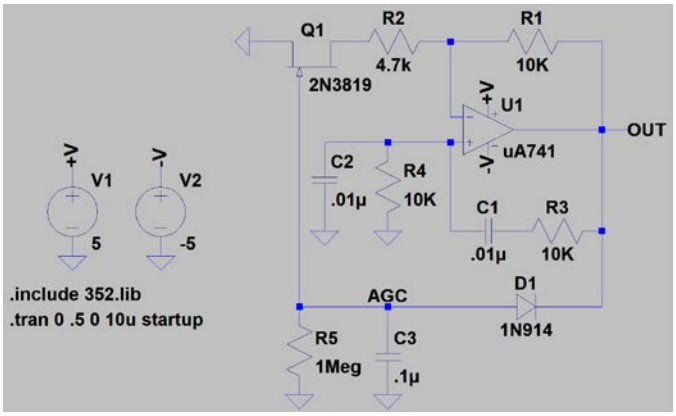


Fig. 1. A Wien bridge oscillator with a self-regulated gain.

High-frequency MHz to GHz oscillators are crucial in radio and wireless communications systems. A Colpitts oscillator is shown in Fig. 2. The transistor amplifier is in the common-base configuration. The capacitor, C_1, shorts the high-frequency signal to the ground. The output is at the collector node. The feedback loop consists of L_1 in parallel with C_2 and C_3 which are in series. The positive, in-phase feedback derived from the output is connected to the emitter node. Two capacitors, C_2 and C_3, determine the feedback factor. Resistors, R_1 and R_2, control and regulate the gain. The resistor, R_3, prevents waveform distortion which starts to occur when the collector voltage falls below the base voltage. Run the simulation. Reduce the inductance by a factor of two. Find how it affects the frequency. Reduce both capacitances, C_2 and C_3, by a factor of two. Find how they affect the frequency. Change R_1 to see its effect on the peak-to-peak voltage.

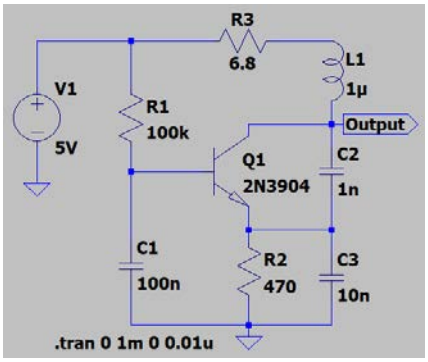


Fig. 2. The circuit diagram of a Colpitts oscillator.

Generating a square wave only requires a positive feedback. Any loop gain, as long as it is greater than unity, is fine. There is no need to subtly balance the gain and the feedback factor. The power supply voltage limits the output. The gain automatically saturates. An astable multivibrator circuit based on two BJTs is shown in Fig. 3. Two conjugate output ports are located at collector nodes of two symmetrically placed transistors. The output of one transistor is ac coupled to the base node of the other transistor and vice versa forming a positive feedback loop. When the first transistor switches to the conducting mode, its collector voltage drops, which, in turn, switches off the other transistor. After being turned off, the second transistor recovers gradually through *RC* charging. Its base voltage rises and eventually switches the second transistor into the conducting mode. This, in turn, switches off the first transistor. The cycle continues forming an oscillator with nearly a square-wave output. Run the simulation, Display the output waveform. Display the waveform at the base node. When the voltage at the base node reaches approximately 0.7 V, the transistor switches on. The voltage at the collector node becomes low. Change the capacitance to adjust the oscillation frequency.

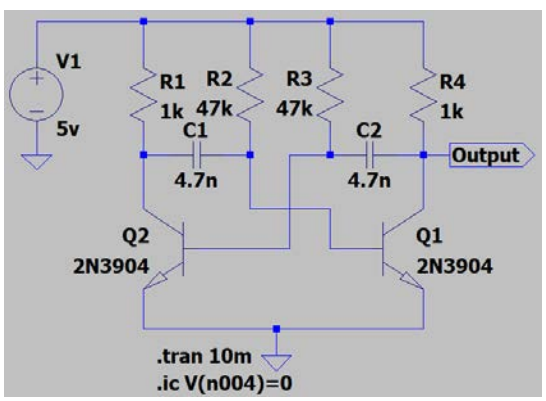


Fig. 3. The astable multivibrator circuit formed by two transistors.

An odd number of inverters can be cascaded to form a ring oscillator. The output of the last inverter is connected to the input of the first inverter. A ring oscillator can operate without any external passive component. The in-phase feedback condition is accomplished when the propagation delay through the inverter chain is one half the period of the oscillation. Each inverter multiplies the signal by a factor of -1. The delay adds another factor of -1. With an odd number of inverters and the delay, the feedback is +1, i.e., in phase. The natural oscillation frequency of the ring oscillator can be modified by adding *R*

and *C* in the circuit as shown in Fig. 4. The *RC* network introduces an additional delay, hence, slows down the ring oscillator. Run the simulation. Display the output waveform. View FFT to find the oscillation frequency. Change the capacitance to see how it affects the frequency.

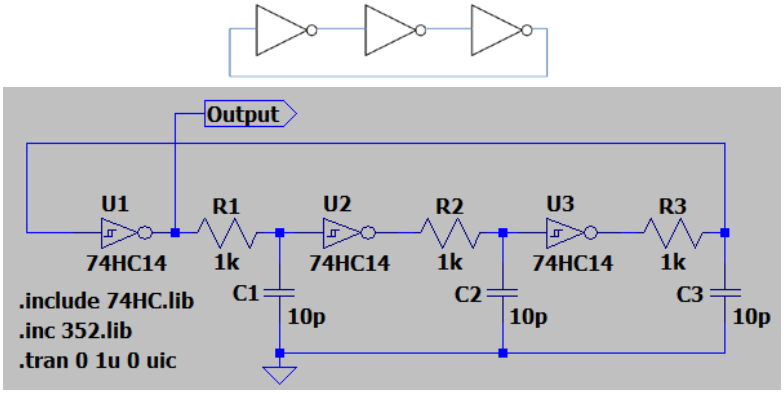


Fig. 4. The symbolic representation of a ring oscillator and its CMOS implementation. Either 74HC00 or 74HC14 can be used. For 74HC00, one must tie the two input nodes together to convert a NAND gate to an inverter. The frequency can be adjusted by loading each inverter with a low-pass filter.

In summary, an oscillator requires an amplifier and a positive, in-phase feedback to operate. The oscillation frequency is determined by the condition that the total phase shift generated by the feedback loop and the amplifier is zero or a multiple of 360^0. As the output builds up, the gain of the amplifier saturates. The output reaches the steady state when the loop gain becomes unity. If the gain saturation is due to the power supply, the output waveform is a square wave. If the amplifier can self-regulate the gain, i.e., lower gain at higher output, the waveform is sinusoidal.

16. Analog Multiplier – Gilbert Cell

Analog signal processing, such as the summation and subtraction, can be accomplished by using an operational amplifier. Can multiplication also be achieved? Indeed, there are circuits and ICs to perform the multiplication of analog signals. In this chapter, we will learn one such circuit, the Gilbert cell, and discuss its applications.

An amplifier generates its ac output by multiplying the input signal with a gain. The gain of a BJT amplifier is current dependent. In principle, by using the second signal to control the current, a BJT amplifier can perform the multiplication. To test this idea, let's examine the differential amplifier circuit shown in Fig. 1. There are two input signals. The 1-MHz voltage source, V_2, is the input signal to be amplified. The 1-kHz voltage source, V_4, controls the current. In simulations, V_4 contains a dc component as the offset and an ac component as the amplitude. The output of the differential amplifier is located at the collector node of Q_2.

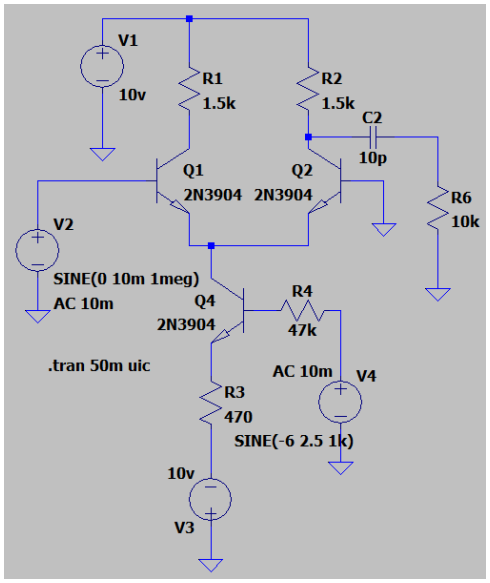


Fig. 1. The circuit diagram of a differential amplifier with a high-pass filter.

Run the simulation. Display the waveform at the collector node of Q_2. Zoom in. The width of the trace, i.e., local swing of the voltage, varies with time at 1 kHz. The width of the trace reflects the ac gain. Indeed, V_4 modulates the gain. However, it not only modulates the ac gain, it also modulates the Q-point voltage. View FFT. The low-frequency peak at 1 kHz corresponds to the modulation of the Q-point voltage. To eliminate the low frequency, there is a high-pass filter consisting of C_2 and R_6 in the circuit diagram. Display

the waveform at the output of the high-pass filter. The waveform clearly shows that the amplitude of the 1-MHz signal is modulated by the 1-kHz signal. View FFT to see the spectrum. There are three peaks: the lower side band at 990 kHz, the center carrier at 1 MHz and the upper side band at 1010 kHz. They form a cluster.

The product of two sine functions is given by: $V = V_1 \cdot V_2 = \sin(\omega_1 t + \theta_1) \cdot \sin(\omega_2 t + \theta_2) = -[\cos(\omega_1 t + \omega_2 t + \theta_1 + \theta_2) - \cos(\omega_1 t - \omega_2 t + \theta_1 - \theta_2)]/2$. As a result of the multiplication, there are two frequencies, the sum frequency and the difference frequency. The sum frequency term represents the up-conversion process in which the signal is shifted to a higher frequency. The difference frequency term represents the down-conversion process in which a high-frequency signal is shifted to a lower frequency. The sum and difference frequencies can be separated by filters.

In addition to the sum and difference frequencies, the circuit shown in Fig. 1 keeps the carrier frequency, i.e., the 1-MHz signal. This single balanced mixer circuit is an amplitude modulator. The circuit shown in Fig. 2 can eliminate the carrier frequency. There are only the sum frequency and the difference frequency at its output. This double balanced mixer is called the Gilbert cell. It is implemented by using transistors in the differential amplifier configuration and a summing operational amplifier. Double balanced mixers can also be implemented by using CMOS or diodes with transformers.

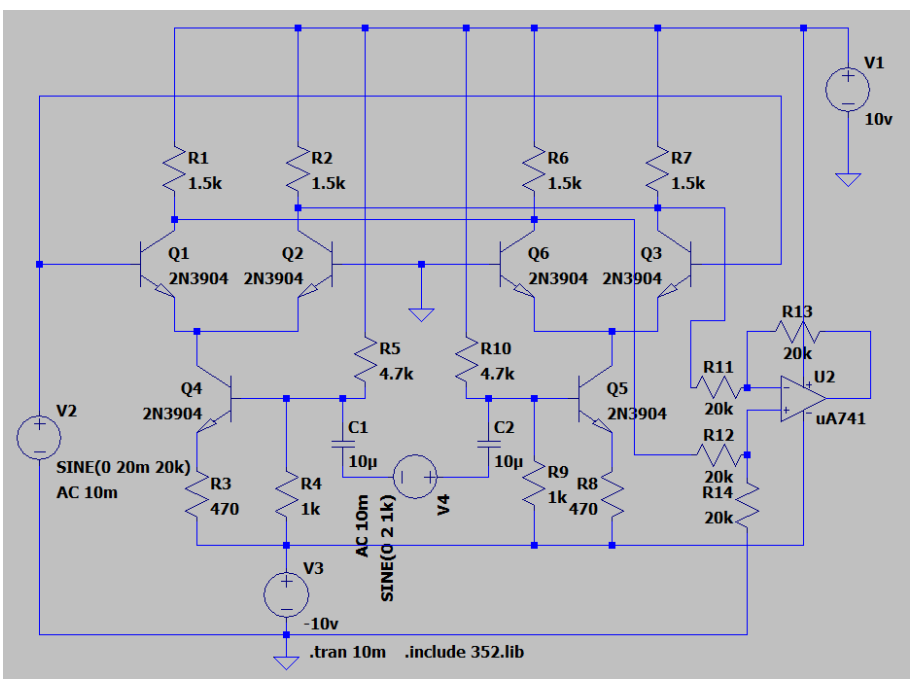


Fig. 2. The circuit diagram of a Gilbert cell.

Display the waveform at the output of the operational amplifier in Fig. 2. Display the spectrum by viewing FFT. Do the frequencies of two primary peaks correspond to the sum and difference frequencies? The higher order peaks are at a much lower power level. If needed, they can be further suppressed by using a filter.

In the real implementation using discrete components on a circuit board, not all transistors are well matched. You can simulate the mismatch by changing the resistance of R_5 slightly. Observe its effect on the output waveform. Please note that V_4 is floating in the circuit diagram. Because of ac coupling using capacitors, the negative side of V_4 can be connected to the ground while implementing the circuit on a circuit board.

When the two frequencies are the same, the difference frequency term yields the phase difference between two signals. The Gilbert cell can function as a phase detector. To see the operation of the phase detector, add a low-pass filter consisting of a 2-kΩ resistor and a 100-nF capacitor at the output of the summing operational amplifier. In the real implementation, change the settings of V_4. Match its frequency to that of V_2. Set the phase angle to 45^0, 90^0, 135^0 and 180^0 in turns. In simulations, set two signal sources to the same frequency and enter a delay time corresponding to the phase angle for V_4. Observe the output of the low-pass filter. The dc voltage correlates with the phase difference.

In summary, we learn how to combine two differential amplifiers and a summing amplifier to form a Gilbert cell. As a double balanced mixer, a Gilbert cell can perform the multiplication of two analog signals. Applications include up conversion, down conversion and phase detection. The up and down conversions are essential to communications systems operating in radio and microwave frequencies.

There are analog multiplier ICs, such as AD834. For readers who are interested in using them, please browse: www.analog.com/media/en/training-seminars/tutorials/MT-079.pdf.

17. Phase-Locked Loop

Timing and synchronization are crucial in many electronic circuits. This applies to the synchronization of analog events to a digital controller. This also applies to the transmitter and receiver in communications systems. The frequency of the analog carrier and the timing of digital clock of the transmitter must be synchronized to those of the receiver. The phase-locked loop is a circuit specifically developed for synchronization. It keeps a locally generated signal at the receiving end in synchronization with the signal sent by the transmitter.

There are three crucial components in a phase-locked loop, namely, a voltage-controlled oscillator, a phase comparator and a loop filter. A voltage-controlled oscillator is a tunable oscillator. Under the control of an applied voltage, it can change its oscillation frequency. A phase comparator compares the phase difference between two input signals. For two digital input signals at the same frequency, an XOR gate provides an output voltage linearly proportional to the phase difference, from 0^0 to 180^0, between them. A loop filter can simply be a low-pass filter.

The circuit diagram shown in Fig. 1 is a phase-locked loop. The circuit provides an opportunity to study how the phase-locked loop operates.

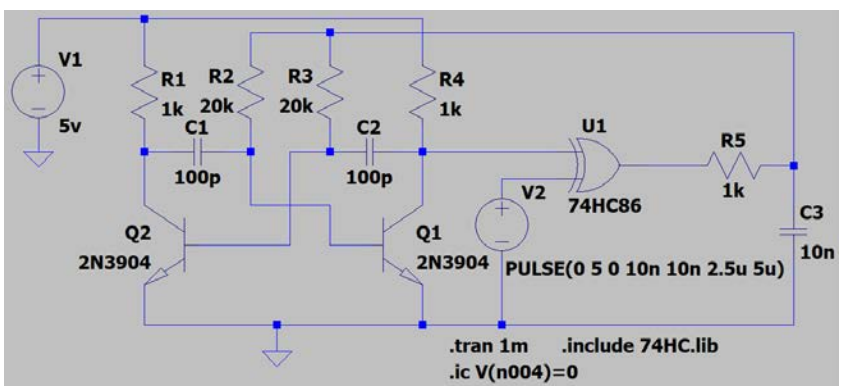


Fig. 1. The diagram of a phase-locked loop circuit. In the circuit diagram, V_2 represents the incoming reference signal.

In the circuit, two 2N3904 transistors form an astable multivibrator. The frequency is controlled by the voltage applied to R_2 and R_3. It is a voltage-controlled oscillator. The XOR gate takes two input signals, the output of a VCO and a reference input clock signal.

It generates an output proportional to the phase difference between the two signals. The drift in the phase difference is tracked by a low-pass filter consisting of R_5 and C_3.

To see the free running frequency, disconnect V_2 from the XOR gate. Replace the connection with a jumper wire connecting XOR to the ground. Run the simulation. Display the waveform at the collector of Q_1. View FFT. What is the free running frequency? (Answer: approximately 190 kHz.)

Simulate the circuit shown in Fig. 1. Display the two input signals of the XOR gate. The output of VCO is synchronized to the reference clock with a phase difference of 90^0 or a time delay of one quarter cycle. Add the waveform from the output of the loop filter. Zoom in to the first 200 µsec. There is a settling time of approximately 100 µsec for the VCO to synchronized to the reference clock signal. Change C_3 to 2.2 nF. Compare the output of the loop filter to the previous setting. What do you observe? (Answer: A larger swing and a faster settling time.) Gradually increase the frequency of the reference clock. Keep the duty cycle at 50%, i.e., the on time is half of the period. Eventually, it will drop out of the 1:1 synchronization. This also happens when the frequency of the reference clock is reduced. The upper bound and the lower bound of frequencies in which PLL can achieve synchronization is the capture range. Within this range, PLL can synchronize to the reference input signal.

Once the PLL is locked onto the incoming reference signal, it can maintain synchronization even when the frequency of the incoming reference signal drifts. How far it can track the incoming signal is called the tracking range. The tracking range is wider than the locking range. In order to find the tracking range, one needs to sweep the reference clock signal. In LTspice, delete the voltage source, V_2. Replace it by a bv voltage source defined by a mathematical formula, e.g., V=2.5*(1+sgn(sin(2*pi*(2e5+1e5*time)*time))). It is a sweeping clock signal. The starting frequency is 200 kHz, which is well within the locking range. The frequency increases at a rate of 100 Hz/msec. To cover a sweeping range of 250 kHz, the stop time for the transient simulation needs to be 2.5 sec. It takes a very long time, therefore, is impractical to simulate. However, when the circuit is implemented on a circuit board, the tracking can be easily observed. Set up the waveform generator to sweep the reference signal. Display two waveforms at the input of the XOR gate. Towards the end of the sweeping cycle, the phase synchronization is lost. The PLL can no longer track the drift of the incoming reference signal. One waveform displayed on the oscilloscope remains steady. The other signal drifts across the screen randomly

indicating that it is out of synchronization with the trigger. One can also sweep down from 200 kHz to 80 kHz to find the locking range on the low-frequency side.

In summary, a PLL contains a VCO, a phase comparator and a loop filter. The output of the loop filter controls the frequency of the VCO. When 1:1 synchronization is achieved, the frequency of the local VCO is exactly the same as that of the incoming reference signal. The two signals maintain a fixed phase relation between them. The performance characteristics of a PLL include the settling time, the locking range and the tracking range. When an incoming reference signal within the tracking range arrives, the VCO can lock onto it after a settling time. Once locked, a PLL can track any slow drift of the incoming reference signal over a broad tracking range. The PLL is essential in analog and digital communications systems.

There are PLL ICs, e.g., CD4046. The datasheet and application notes discuss detailed characteristics of the device. In a CD4046, there are two phase comparators. The first one is an XOR gate. Readers may explore how the second phase comparator behaves. The reference incoming signal is not always a perfect clock signal. For example, readers may explore whether a PLL can recover the clock signal from the output of a pseudorandom number generator.

There are tutorials of PLL on YouTube. Readers may also find tutorials online, e.g., https://www.bharathuniv.ac.in/downloads/ece/HEMA-LIC/introduction%20to%20PPL-HEMA.pdf.

18. Modulation and Detection Circuits

In communications systems, electromagnetic waves carry the information. To transmit binary digital information, two amplitude levels, on and off, two frequencies, f_1 and f_2, or two phase angles, 0 and 180^0, represent H and L, respectively. They modulate the sine wave carrier. Such modulation schemes are call amplitude shift keying (ASK), frequency shift keying (FSK) and binary phase shift keying (BPSK). In this chapter, we will study circuits for modulation and detection. In general, the carrier wave has a frequency in the radio and microwave region, i.e., MHz to GHz. The baseband information used to modulate the carrier has a much lower bandwidth in the kHz to MHz range.

To perform ASK, an analog switch is needed. It turns on or off the sine wave carrier. There are ICs, including high speed CMOS devices, to perform such a task. The circuit shown in Fig. 1 is a simple BJT analog switch. The positive power supply is replaced by the sine wave carrier with both positive and negative voltages. When its voltage is positive, the transistor functions normally in the common-collector configuration. When the voltage is negative, the roles of emitter and collector are reversed. The transistor can be considered to operate in the common-emitter configuration but with deteriorated characteristics. In both configurations, a positive base voltage switches on the transistor. A negative voltage switches off the transistor. Run the simulation. Display the digital input signal and the output waveform to see the ASK circuit in operation. Adjust the resistance of the base resistor to see how it affects the output. For example, when you decrease the base resistance, what happens to the output waveform? (Answer: The negative portion of the waveform becomes bigger.)

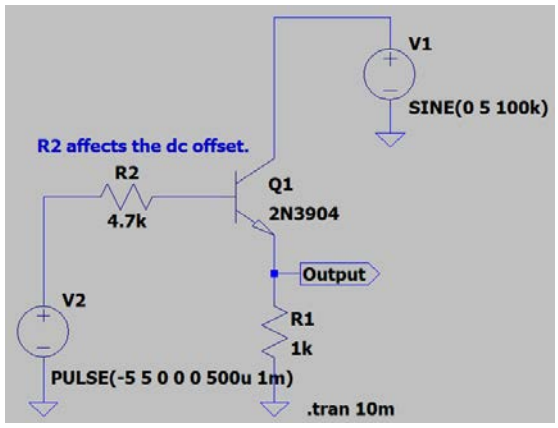


Fig. 1. The circuit diagram of an ASK modulator.

Detection of the ASK signal can be accomplished by using a signal diode as a rectifier shown in Fig. 2. The signal diode passes through the positive portion of the ASK waveform and charges up the capacitor. The capacitor filters the ripple at the carrier frequency. A resistor, R_3, discharges the capacitor to enable the baseband signal to go through.

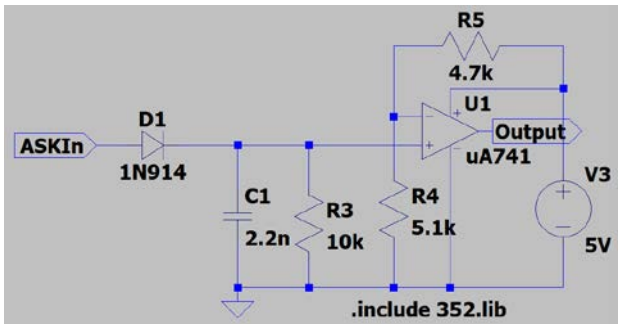


Fig. 2. The diagram of an ASK detection circuit. The signal diode rectifies the ASK signal. The level comparator recovers the binary information.

Connect two circuits in Figs. 1 and 2 together. Run the simulation. Display the waveform at the output of the signal diode. There is still a substantial amount of ripple at the carrier frequency. Adjust the capacitance to see how it affects the rising edge of the ripple. Adjust the resistance to see how it affects the trailing edge of the ripple. To completely eliminate the ripple, a level comparator circuit is needed. Adjust the decision level by varying one of the two resistors biasing the inverting input node of the operational amplifier to obtain a clean digital output signal.

The circuit shown in Fig. 3 generates the FSK signal. It is a loaded ring oscillator. An additional capacitor under the control of a switching transistor is used to modulate the oscillation frequency. Run the simulation. View FFT. There are two peaks corresponding to f_1 and f_2. What are the frequencies? (Answer: 23.5 kHz and 27.5 kHz.)

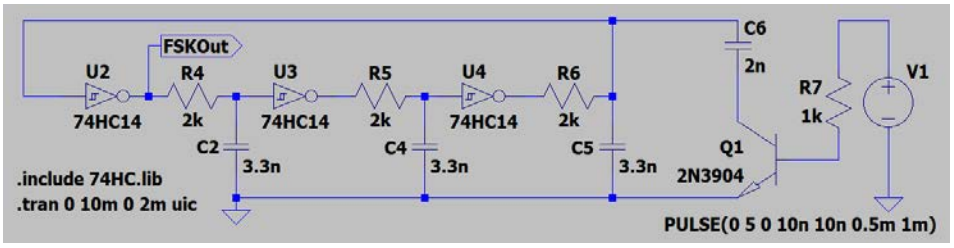


Fig. 3. The circuit diagram of an FSK modulator. It consists of a ring oscillator and a switching transistor.

To detect the FSK signal, a PLL IC, CD4046, is used as shown in Fig. 4. There are two resistors, R_1 and R_2, controlling the frequency range. The output of the phase comparator is located at the PC1out port. The externally connected R_3 and C_3 form the first low-pass filter. Its output is connected to VCOin to control the frequency of the local oscillator. The second low-pass filter consisting of R_8 and C_7 reduces the ripple at f_1 and f_2 to make the baseband at 1 kHz dominant. The level comparator recovers the baseband information. Combine both circuits in Figs. 3 and 4. Run the simulation. Display waveforms at SigIn and VCOout. Is the output of VCO synchronized to the output of the ring oscillator? (Answer: Yes.)

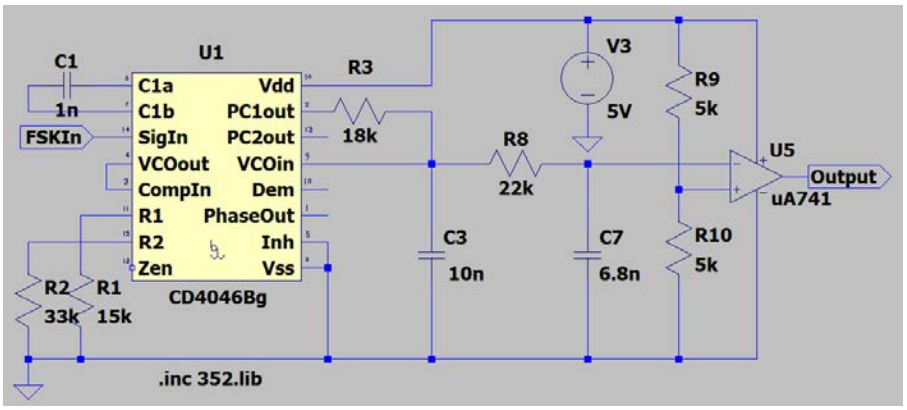


Fig. 4. The circuit diagram of an FSK detection circuit based on a PLL IC.

To generate the BPSK signal, we need a circuit which can modulate the phase angle of the carrier. An 180^0-phase shift is equivalent to multiplying the carrier by -1. The double-balanced mixer, e.g., a Gilbert cell, is a multiplier. The circuit diagram shown in Fig. 5 can perform BPSK. A differential digital signal modulates the constant current sources. Run the simulation. Display the output waveform. Zoom in to see the abrupt phase change during switching. Please note that V_4 in the circuit diagram is floating from the ground. It is fine for simulations. The circuit can't be physically implemented as is using a normal waveform generator. It requires a special waveform generator with a differential drive circuit at its output.

Detection of BPSK can be accomplished by summing the BPSK signal and a synchronized local carrier of equal amplitude. In the circuit diagram shown in Fig. 5, this is done symbolically by using a voltage source generating a signal defined by a mathematical function. When the phase angle is 180^0, the summation yields zero. When the phase angle is 0^0, the summation yields twice the amplitude. Run the simulation.

Display the waveform at the output of the summing voltage source, B_1. The waveform is the same as an ASK signal. An envelope detector can recover the baseband information.

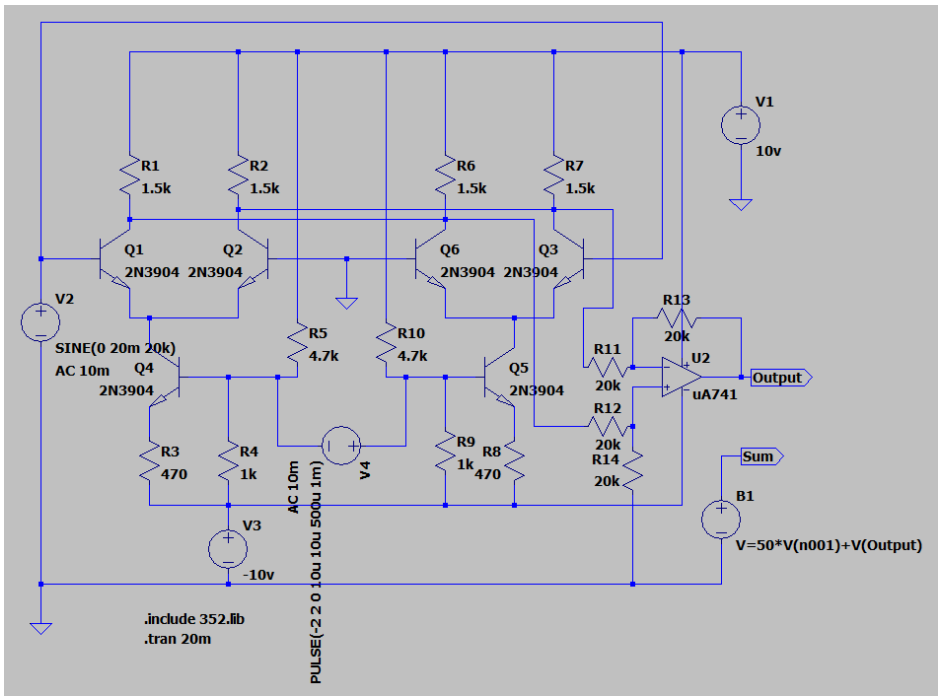


Fig. 5. The circuit diagram of a BPSK modulator and detector. The Gilbert cell provides the modulation. The modulated signal appears at the "Output" port. A summing amplifier symbolically represented by B_1 demodulates the BPSK signal and recovers the baseband information. In the formula defining B_1, the voltage at the base node of Q_1 is V(n001). The output of the summing amplifier is located at the "Sum" port.

In this chapter, we discuss circuits of three digital modulation schemes, namely, ASK, FSK and BPSK. To detect and recover the ASK information, an envelope detector is used. This direct detection method involves no locally regenerated carrier wave. It is an incoherent detection scheme. To detect the FSK information, a PLL IC is used. The signal driving the voltage-controlled oscillator contains the information. To detect BPSK, a regenerated carrier wave is needed. It belongs to the coherent detection scheme. It is the most sensitive method for detection in communications systems.

19. Infrared Transmitter and Receiver

Optoelectronic devices are critical components in control and communications systems. In this chapter, we learn characteristics of a light emitting diode (LED) transmitter circuit and a photo-transistor receiver circuit. Together, they can establish an optical link.

Many systems nowadays rely on optoelectronic components. Examples include fiber optics, CD/DVD, Blue Ray, remote control, power electronics and smart grid. The scroll wheel of a computer mouse has slots located between a pair of optical transmitter and receiver. Light can pass through slots as the wheel rotates. By counting the number of slots, scrolling is tracked. A packaged LED and photo-transistor pair functions as an opto-isolator. It can provide protection between the low-voltage control circuit and the high voltage, power electronics. Knowing how to design circuits to interface with optoelectronic components is important.

Optoelectronic components in remote control and opto-isolators operate in the near infrared region with a wavelength of 880-940 nm. Examples include QED123, a GaAs infrared LED, and QSD123, a Si photo-transistor. An LED or diode laser operates like a p-n junction diode. The voltage at which an infrared LED begins to conduct is around 1.0 to 1.2 V. Visible LEDs operate at higher junction voltages. Although higher current leads to higher optical power, an LED can only sustain a maximum current of approximately 30 mA except high power devices. Make sure that the LED current does not exceed its limit in the physical implementation. A photo-transistor is similar to a BJT transistor. However, the base has no contact lead. The base region absorbs photons and generates a photo current. The photo current is amplified to become a much larger collector current. The maximum V_{CE} placed across the photo-transistor should not exceed 15 V in the implementation. The optical beam propagates from the LED to the photo-transistor through the air. The beam diverges and the power gradually diminishes. The detected signal depends on the alignment and distance between the infrared LED and the photo-transistor detector.

The pin configurations of LED and photo-transistor are shown in Fig. 1. The shorter pin is the cathode of LED or the emitter of a photo-transistor. Current flows from the anode to cathode in the LED and from collector to emitter in the photo-transistor. Hence, a positive voltage should be applied to the anode of LED and the collector of the photo-transistor. Do not reverse bias any optical component because it can be damaged easily.

While designing your circuit, make sure that the current and voltage limits specified in the datasheet are not exceeded.

Fig. 1. Infrared LED and photo-transistor. Light is emitted or detected through the round tip. Dark plastic enclosure filters out the visible ambient light.

In the LTspice optos library, there are optical isolators, e.g., PC817. They contain an LED and a photo-transistor pair forming an optical isolator. We use it is the circuit diagram simply because the device is available in the LTspice library. Similar to the characterization of a rectifying diode, one can obtain the static *I-V* characteristics of the LED. According to the simulated *I-V* curve, the diode operates with a voltage, V_{LED}, around 1.06 V. To study the dynamic characteristics, put together the circuit shown in Fig. 2. Run the simulation. Display the current of the LED. Display the output voltage at the emitter node of the photo-transistor. The response of LED is very fast. The current of LED even shows a transient spike. The speed of the photo-transistor limits the overall response. Its rise time and fall time are around 2 µsec. Reduce the voltage of the input signal to 2 V. Increase the resistance of R_3 to 1 kΩ. Display the waveforms. What is the effect of a higher load resistance to the transient response? (Answer: A higher load resistance leads to a slower response.)

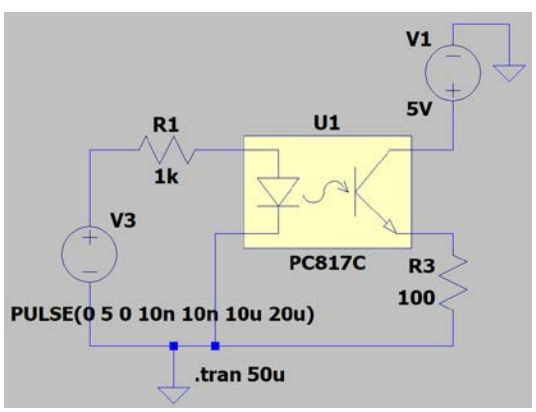


Fig. 2. The circuit diagram for characterizing the transient response of an opto-isolator.

The diagram of a complete circuit including the LED driver and the transimpedance amplifier for the photo-transistor is shown in Fig. 3. You may design your own circuit. For

example, you may a common-collector LED driver and a BJT amplifier for the detector. The transimpedance amplifier converts input photocurrent to an output voltage. The photo-transistor is biased by a positive power supply voltage at its collector. Its emitter is connected to the inverting input of the operational amplifier. Since the non-inverting input is connected to the ground, the emitter of the photo-transistor is virtually grounded. Photocurrent flows through the feedback resistor of the operational amplifier to generate the output voltage. The value of the feedback resistor is determined by the desired sensitivity or ratio of the output voltage and the photocurrent. For example, when the feedback resistor is 1-kΩ, the transimpedance amplifier generates 1 V per 1 mA. You can decrease the feedback resistor to get a lower gain. How does the gain affect the bandwidth?

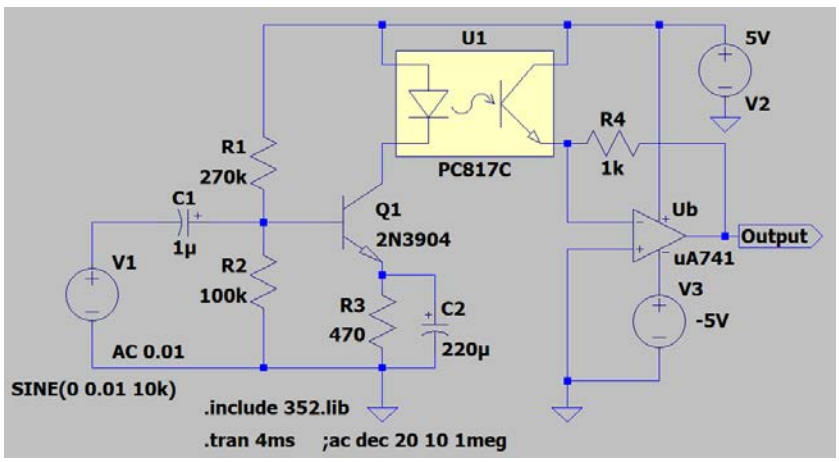


Fig. 3. The circuit diagram of an optical link. The driver for the LED is a common-emitter BJT amplifier. The current of the photo-transistor goes through a transimpedance amplifier circuit to generate the output.

Run the simulation. Display the current of the LED and the output voltage of the trans-impedance amplifier. Adjust the dc bias of Q1 by changing the resistance of R_1 to optimize the bias condition of the LED for a large swing without distortion. Change the amplitude of V_1 if needed. Obtain the Bode plot. Since there is a spike in the transient response of the LED, there is likely a peak at high frequency in the Bode plot. You can add a capacitor in the 100 pF to 10 nF range in parallel to the LED to suppress the high-frequency response.

In this chapter, we learn the characteristics of two optoelectronic devices, namely, LED and photo-transistor. They can form an optical link. Such a link can provide electrical isolation between the transmitter and the receiver. It is immune to electrical interference.

20. Electrocardiogram

The purpose of this chapter is to explore biomedical electronics. We will study an electronic circuit based on an instrumentation amplifier. The circuit is capable of detecting the electrocardiogram (ECG) signal.

Biomedical instrumentation is a vital part of health care. Imaging systems are used extensively for diagnosis. Electrical signals can monitor activities of nerves. Heart muscles pump blood in a highly coordinated manner under the stimulation of electrical signals emanating from the sinoatrial node. Such signals are small, i.e., in the mV range on the skin. The noise in the environment, noticeably the 60-Hz power line noise, is large. It can be very challenging to uncover a small signal buried in a large background noise. For an introduction, browse http://www.medicine.mcgill.ca/physio/vlab/cardio/introECG.htm.

Instrumentation amplifier offers a very large common-mode rejection ratio (CMRR). It can differentially amplify a small signal while suppressing the common noise present at its two input nodes. Let's consider the circuit diagram shown in Fig. 1. IC chips in the diagram include one instrumentation amplifier and two operational amplifiers.

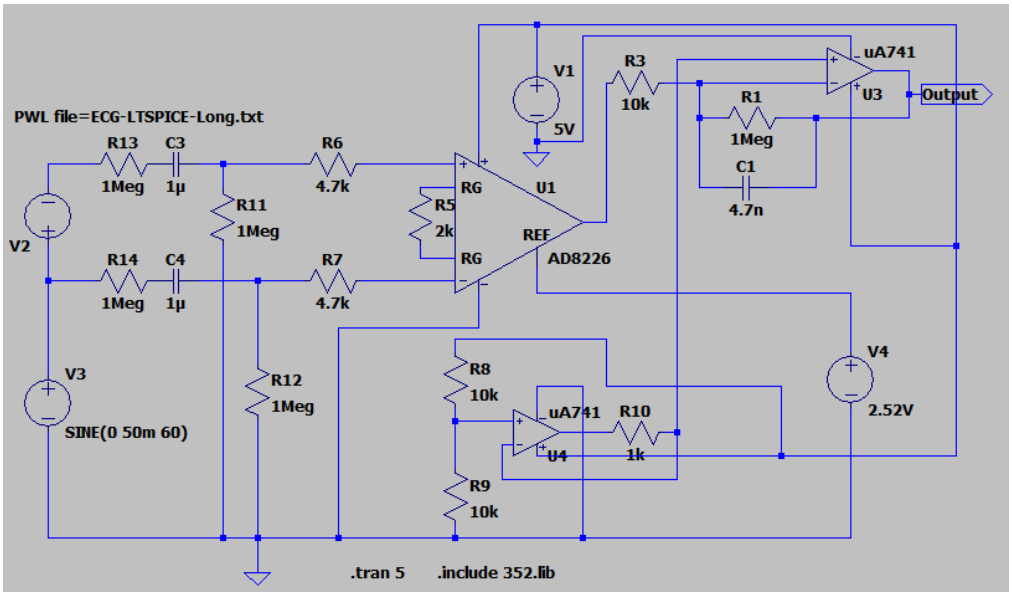


Fig. 3. The diagram of an ECG circuit. The 60-Hz common-mode noise is represented by V_3. The small ECG input signal is represented by V_2. Its waveform is specified in a text file. The dc voltage source, V_4, is for testing only. In the physical implementation, it is replaced by an active filter to compensate for the slow drift.

The center of the circuit is the AD8226 instrumentation amplifier. It has a CMRR >90 dB. In the circuit, there are two ac signal sources. The 60-Hz sine wave noise is connected to the inverting input node of AD8226. The 60-Hz sine wave and a small ECG signal are connected to the non-inverting input node of AD8226. The 60-Hz sine wave represents the ac power line noise. It is a common input to both the inverting and the non-inverting input nodes. Only the ECG signal is the differential input. The ECG waveform is defined in a text file. The file is included in the LTspice customization package. In the file, there are 880 data points. Each data point is defined by a pair of time and voltage values. The total duration is approximately 5 sec. The peak-to-peak voltage of the ECG signal is 2.37 mV. The peak-to-peak voltage of the 60-Hz noise is 100 mV. Two resistors, R_{13} and R_{14}, represent the contact resistances of the skin, one at each electrode. Two capacitors, C_3 and C_4, are coupling capacitors. The two resistors, R_{11} and R_{12}, provide the discharge path for the coupling capacitors. There are two protection resistors, R_6 and R_7.

The gain of the instrumentation amplifier is controlled by a single external resistor, R_5. According to the datasheet, the differential gain G=1+49.5 kΩ/R_5. The instrumentation amplifier has a reference input node. To learn what the reference input node does, a dc power supply with an adjustable voltage is used. In the actual implementation, it is driven by an active filter to compensate for any slow drift in the baseline voltage. The ECG waveform with a limited frequency is superimposed on the baseline voltage. A low-pass operational amplifier is used to suppress the high-frequency noise. It also provides a gain to generate an output signal with a peak-to-peak voltage of few volts. Since there is only one power supply, the non-inverting input node of the operational amplifier needs a +2.5 V bias at its input. It is provided by the operational amplifier, U_4, serving as a buffer.

Run the simulation. Display waveforms at the non-inverting input node of AD8226, the output node of AD8226 and the output of U_3. Can you see the ECG signal at the input node of AD8226? Can you see it at the output of AD8226? Increase the amplitude of the 60-Hz signal to 1.5 V. Run the simulation again. Can you see the residual 60-Hz noise at the output of AD8226? Please note that the peak-to-peak voltage of the ECG signal at the input is only 2.37 mV. The superior CMRR of the instrumentation amplifier is very effective in suppressing the 60-Hz noise. Bring down the amplitude of 60-Hz noise back to 50 mV. Adjust R_5 to a lower resistance to see how it controls the gain. Adjust the dc voltage of V_4 by a small amount, e.g., ±15 mV, to see how it controls the baseline voltage. To simulate the low-frequency drift, you can also change V_4 to a 0.2-Hz sine wave with a dc offset of 2.52 V and an ac amplitude of 15 mV. The reference input of the

instrumentation amplifier facilitates the compensation of baseline drift in the actual implementation. It is driven by an active filter similar to U_3 but with a longer $R{\cdot}C$ time constant, i.e., a lower -3 dB frequency.

To understand how critical the contact electrodes are, two resistors, R_{13} and R_{14}, are incorporated into the circuit diagram. The resistance emulates the contact between the electrode and the skin. Change the resistance of R_{13} to 900 kΩ. It creates an imbalance between the two input nodes of the instrumentation amplifier. The 60-Hz ac noise is no longer in the purely common mode. Observe the output at the low-pass operational amplifier. The signal contains a substantial amount of the 60-Hz noise. In measuring ECG, electrodes are covered by a conducting jelly to ensure a solid contact with the skin.

In this chapter, we learn how an instrumentation amplifier operates. We also learn the importance of establishing good electrode contacts in biomedical or other high impedance measurements. For physically implementation, use the circuit shown in Fig. 4. The operational amplifier U_2 tracks and compensates the slow drift.

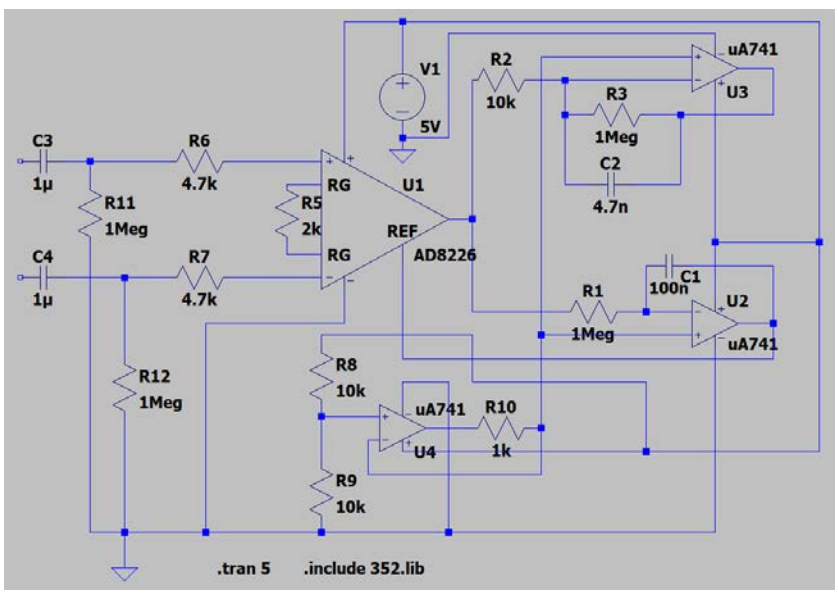


Fig. 4. The diagram of an ECG circuit with an integrator to compensate for the drift. Electrodes are connected to the circuit through two capacitors at the left side. Instead of 741s, one can use an OP482 chip containing four operational amplifiers.

Acknowledgment

The waveform of the ECG included in the LTspice customization package was derived from https://www.instructables.com/Simulated-ECG-Signal-Acquisition-Using-LTSpice/.

21. AC Power Circuits

The power grid in North America transports electricity with 60-Hz ac. In this chapter, we will study device and circuits relevant to the control and generation of ac power. Circuit diagrams are intended for simulations only because ac voltage is high, hence, can be hazardous.

To control the ac power, semiconductor devices, such as SCR and triac, are used. SCR has a pnpn or npnp structure. It can conduct during the positive half cycle and rectify ac like a diode. However, different from a diode, the current doesn't flow when a forward bias is applied alone. It can hold off a large forward bias until a gate pulse arrives. By controlling the timing of the gate signal, one can control when the current starts to flow during each ac cycle, hence, the amount of power delivered to the load. A triac operates in the same manner but is bi-directional. It can switch during both positive and negative half cycles.

The device, 2N5062, is a SCR. It has three terminals. The ac power goes through the load before reaching the anode. The cathode is connected to the ground. A control pulse synchronized to the 60-Hz ac but having an adjustable delay is connected to the gate. The graph of SCR characteristics reproduced from the datasheet is shown in Fig. 1.

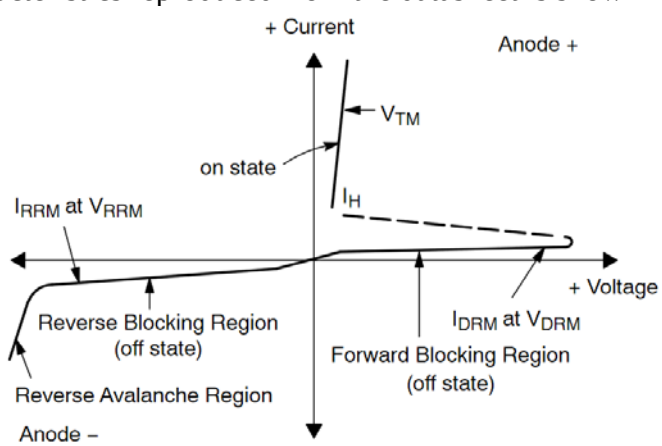


Fig. 1. The qualitative I-V characteristics of SCR.

Under a forward bias, the SCR operates in two states: the off or blocking state with a low current and the on or conducting state with a low voltage. Before the gate signal arrives, the ac power is blocked by a high forward breakdown voltage. When a gate pulse arrives, the SCR starts to conduct with a low forward voltage like a rectifying diode. Once the SCR

is switched to the conducting state, it continues to conduct until the current falls below the holding current. The SCR is then reset to the blocking state. During the negative half cycle, SCR operates in the reverse blocking region. The switching from off to on then back to off occurs in each and every ac cycle. The duration of the on time is controllable by adjusting the arrival time of the gate pulse.

To visualize how SCR operates, draw and simulate the following circuit diagram. The SCR, 2N5062, is in the 352 library. In the circuit, the ac power source is represented by V_1. It operates at 60-Hz, 12-V (RMS). The gate pulse is generated by V_2. It is synchronized to the 60-Hz ac but with an adjustable delay. The rise and fall time and the duration of the gate pulse are not critical. Only the delay time is critical. In the circuit diagram, both the rise time and fall time are 10 nsec. The pulse height is 5 V. The duration of the gate pulse is 10 µsec. The delay shown in the diagram is 4 msec. You need to adjust the delay.

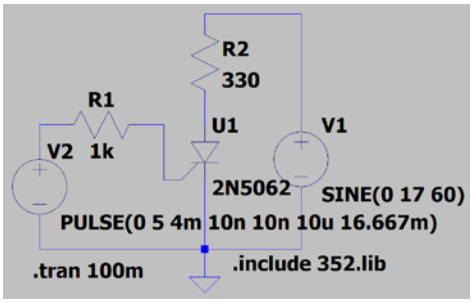


Fig. 2. The SCR test circuit.

Display voltage waveforms at the anode and the gate of SCR. Display the current going through the load resistor, R_2. You can clearly see that the current starts to flow when the gate pulse arrives. Adjust the delay to see how a longer delay reduces the amount of power delivered to the load. Power is delivered to the load only when SCR carries a current. A shorter delay increases the amount of power delivered to the load. Adjust the duration of the gate pulse to verify that it has no effect on the power delivered to the load.

A complete SCR control circuit requires a pulse sequence with an adjustable delay synchronized to the sinusoidal ac signal. One can use a monostable device, such as 74HC123, to control the delay. However, the simulation of 74HC123 runs very slowly in LTspice. An alternative approach is to use the 555 timer IC as shown in Fig. 3. This circuit is derived from a webpage of the Electronic Design News: https://www.edn.com/555-timer-triggers-phase-control-circuit/.

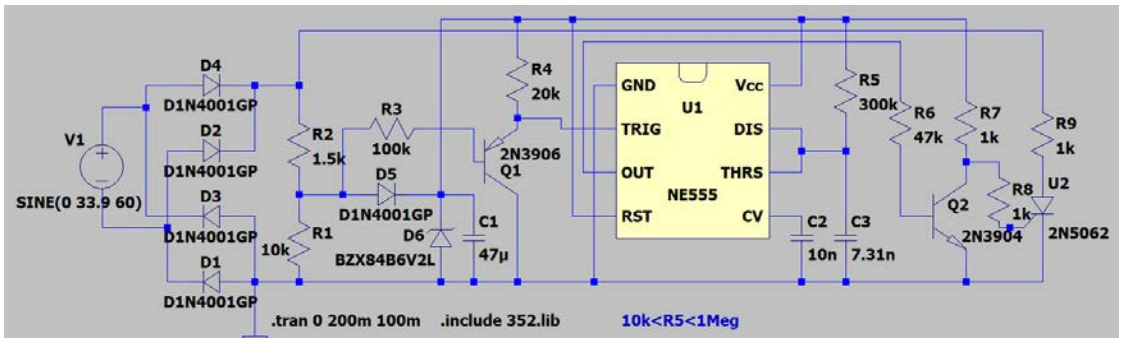


Fig. 3. The complete SCR control circuit.

In the circuit diagram, V_1 represents the output of a 24-V ac transformer. The full-wave rectifier inverts the negative half cycle of ac to positive. Resistors, R_1 and R_2; rectifying diode, D_5; Zener diode, D_6; and capacitor, C_1, form a low-voltage, dc power supply. It provides 6 V dc to power the control circuit. The transistor, Q_1, is a buffer amplifier. It provides a downward pulse to trigger the 555 timer IC into action. The 555 IC operates in the monostable mode. It generates synchronized pulses with an adjustable duration determined by R_5 and C_3. The duration of the monostable pulse translates into a delay. At the trailing edge of the monostable output, the SCR starts to conduct. Since SCR needs a positive gate pulse, transistor Q_2 operates as an inverter. Compose the circuit. Run the simulation. Display waveforms at the output of the full-wave rectifier, the collector node of Q_2 and the current of R_9, which is the load resistor. Change the resistance of R_5 from 10 kΩ, 100 kΩ, 470 kΩ, 680 kΩ to 1MΩ. This will adjust the delay, hence, the amount of power delivered to the load.

Solar panels play an important role in the quest for renewable energy. Solar panels generate the electricity in dc. To be compatible with the distribution grid, solar panels need an ac inverter to convert the dc to ac. A simple example of ac inverter circuits is shown in Fig. 4.

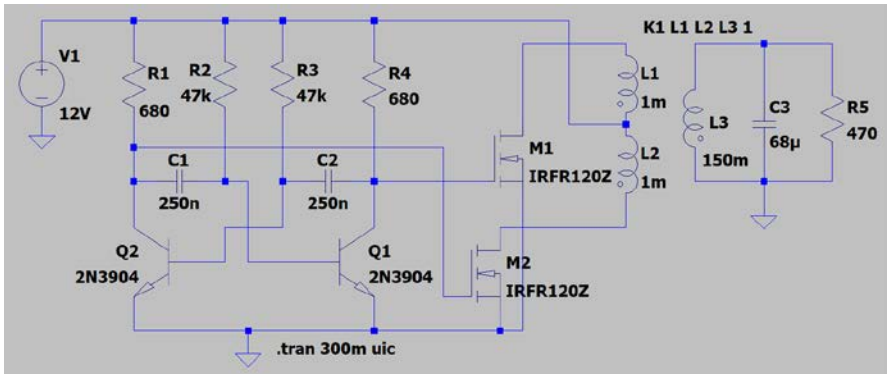


Fig. 4. An ac inverter circuit. The transformer has a unity magnetic coupling factor, *K1*.

This circuit consists of an astable multivibrator and a transformer. The multivibrator generates a square wave at 60 Hz by choosing *R* and *C* values. The two output signals at collector nodes switch on the power MOSFETs in turns to actuate the primary winding of the step-up transformer with a center tap. The dc power supply voltage and the number of turns in the primary and secondary windings determine the output ac voltage. Since the input is a square wave, the native output of the transformer is also a square wave. To reduce the harmonics, a capacitor is attached to the secondary winding. Simulate the ac inverter. Display waveforms at the gate nodes of the power MOSFETs and the output of the secondary winding. Adjust the capacitance of C_3 to see its effect on the shape and amplitude of the waveform. View FFT to see the harmonics. Change the value of L_3 which is the self-inductance of the secondary winding to see its effect on the output voltage. The self-inductance correlates with the number of turns of the winding. Change the value of R_5 to see whether the output voltage varies with the load. An ideal ac inverter should generate a sine wave. The circuit shown in Fig. 4 demonstrates the operational principle of ac inverters. It is not ideal. To generate an ideal sinusoidal ac output, the oscillator needs to be sinusoidal. The output voltage of a well-built ac inverter should be steady against change in the load current.

In summary, there are electronic devices and circuits designed to control the ac power. For example, SCR and triac can control the amount of power according to the arrival time of the gate pulse. AC inverter circuits consisting of an oscillator and a transformer can convert electricity from dc to ac.

22. DC Motor Control Circuits

In this chapter, we will explore how to find circuits for design projects. Motors are essential to many applications, such as control, robotics, drones, etc. In a design project of robotics, one needs driver circuits for motors. The traditional approach is to look into handbooks of electronic circuits. A handbook of electronics may contain more than one thousand pages of circuit diagrams. Nowadays, the internet has become an alternative resource. Search the web using key terms, such as dc motor, motor control circuit and LTspice motor control. You will find following webpages:

www.electronics-tutorials.ws/io/io_7.html

www.precisionmicrodrives.com/content/ab-025-using-spice-to-model-dc-motors/

courses.engr.illinois.edu/ece110/sp2020/content/labs/Experiments/Simulation Lab 6 - DC Motor.pdf

www.electronicsforu.com/electronics-projects/dc-motor-speed-controller

Read the information posted on these websites. You will find how motors work, their electrical characteristics and how to simulate a motor in LTspice. Following the instruction on the Illinois.edu website, the schematics and the symbol of a motor have been downloaded and included in the zip file for customizing LTspice. While drawing circuits, you can find the motor component in the 352 library.

To vary the speed of a dc motor, one needs to control its current. The simplest approach is to use a common-collector amplifier. Draw and simulate the circuit shown in Fig. 1. The

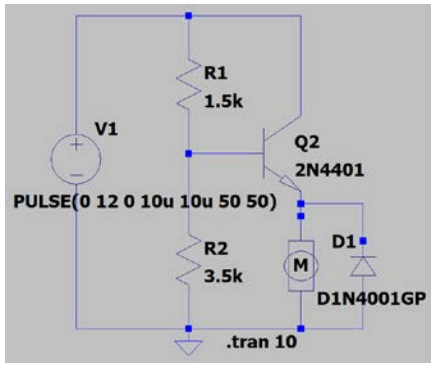


Fig. 1. An analog driver circuit for a dc motor. Instead of a transistor, a Darlington pair can be used for high power motors. The pulse voltage source emulates the dc power supply and a switch which is turned on at time zero.

two resistors, R_1 and R_2, represent the two arms of a 5-kΩ potentiometer. The wiper pin is connected to the base node. By adjusting the position of the wiper pin, one can control the speed of the dc motor. The diode provides protection against the back-EMF generated by the motor during transient switching.

An alternative approach to control the speed of a dc motor is to use the pulse-width modulation (PWM). The dc motor drive operates in the pulse mode. The motor turns faster at a high duty cycle and slower at a low duty cycle. The circuit diagram shown in Fig. 2 is a PWM circuit. The 555 timer IC operates as an oscillator. The two resistors, R_1 and R_2, represent the two arms of a 50-kΩ potentiometer. Along with D2, the potentiometer controls the duty cycle. The low-pass filter consisting of R_4 and C_2 shields the IC from any transient spike. An n-channel MOSFET in the LTspice library is arbitrarily chosen as the driver. To protect the transistor from the back-EMF, D1 is incorporated into the circuit.

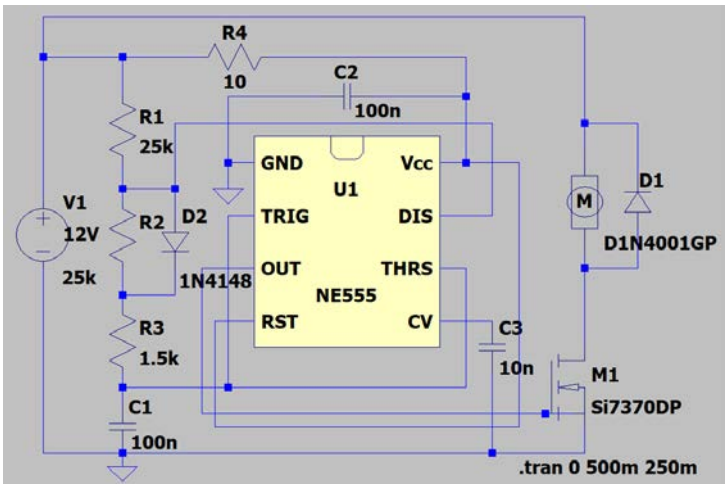


Fig. 2. A dc motor speed control circuit using pulse width modulation.

Simulate the circuit. Display the gate voltage of the MOSFET and the current of the dc motor. Adjust R_1 from 1 kΩ to 49 kΩ while keeping the total resistance of R_1 and R_2 fixed at 50 kΩ. This will keep the frequency of the oscillator constant. A larger R_1 leads to a higher duty cycle. Adjust the duty cycle to approximately 50%. Display the voltage at the drain node of the MOSFET. Watch the peak voltage. Disconnect D1 to disable the protection against the back-EMF. Run the simulation again. Display the drain voltage. Do you observe a very large spike when the motor is turned off? The protection diode is crucial in circuits with an inductive load.

DC motors can turn in both directions. To operate a motor in both the forward and the backward direction, an H-bridge circuit shown in Fig. 3 is used. This is a simplified H-bridge circuit. Both the control and the motor operate with a 5-V power supply. Transistors Q1 and Q4 form a pnp and npn complementary pair. Transistors Q2 and Q3 form the second pair. Under the control of input logic signals, one pair is turned on at a time. For example, when both the A input and the B input signals are H, transistors Q2 and Q3 conduct. The motor turns in one direction. When both input signals are L, Q1 and Q4 conduct. The motor turns in the other direction. Draw and simulate the circuit. Change the logic input. Display the current of the motor to verify the bidirectional operation. To control motors operating at a higher dc voltage, there are H-bridge modules compatible with the Arduino Uno which is a popular microcontroller for design projects.

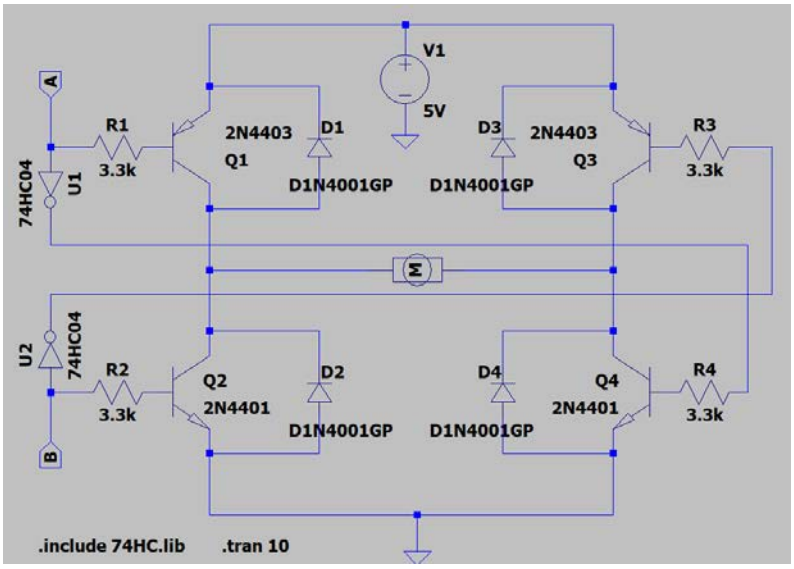


Fig. 3. A bidirectional motor driver circuit.

In summary, this chapter serves as an example demonstrating how to come up with circuits not encountered before. The first step is to look for examples and identify the operational principle. Then, you can design your own circuits or choose from available modules to meet the requirements. Although there are numerous circuits for all kinds of applications, knowing fundamental circuits establishes a solid foundation for electronic circuit design.

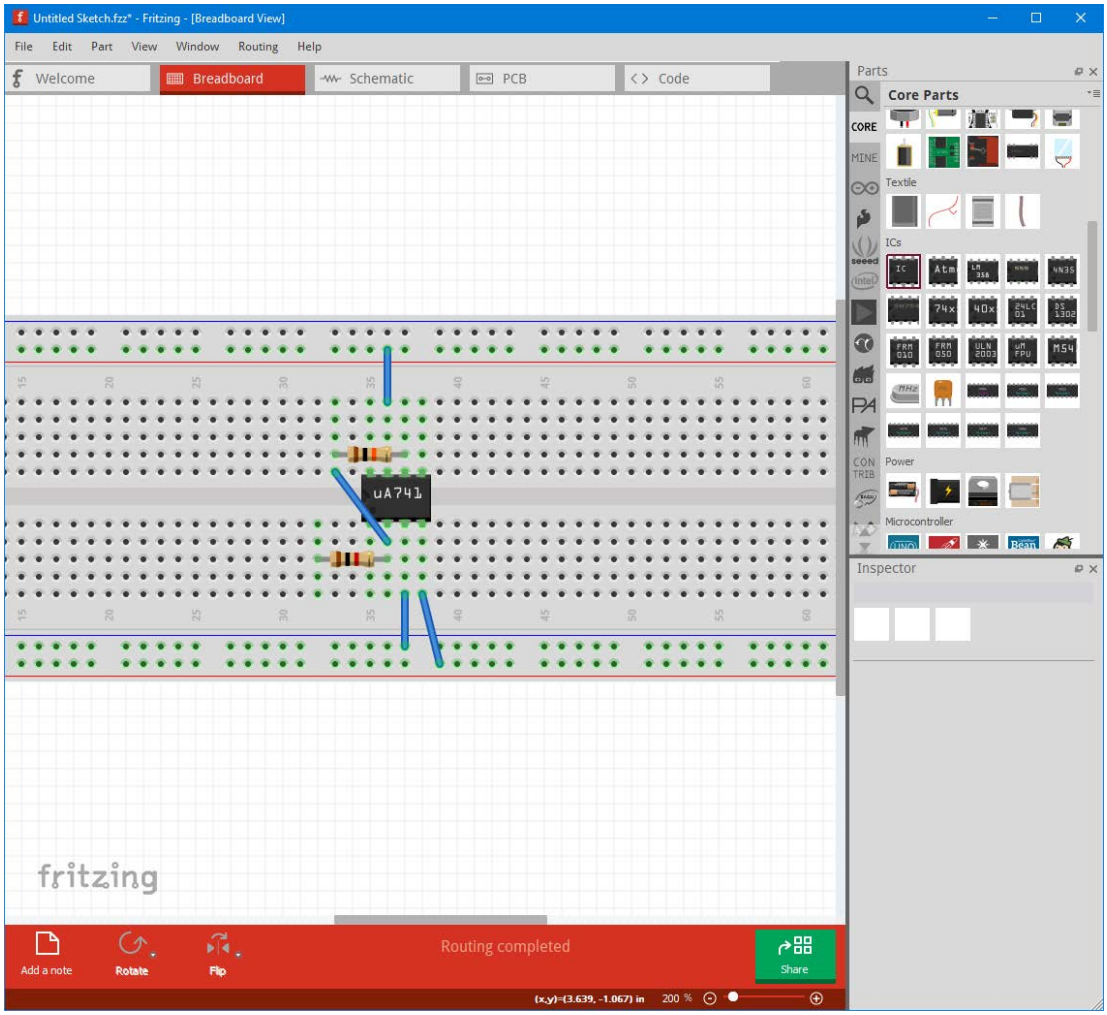
Appendix A Frequently Used Units and Symbols in Electronics

Unit	Symbol
Ampere (current)	A
Coulomb (charge)	C
cycle per second (frequency)	Hz
decibel (relative power)	dB
degree Celsius (temperature)	^{o}C
electronvolt (energy)	eV
Farad (capacitance)	F
femto, 10^{-15}	f
giga, 10^{8}	G
Henry (inductance)	H
Kelvin (absolute temperature)	K
kilo, 10^{3}	k
Mega, 10^{6}	M
Mho (inverse resistance)	Ω^{-1}
micro, 10^{-6}	μ
milli, 10^{-3}	m
nano, 10^{-9}	n
Ohm (resistance)	Ω
pico, 10^{-12}	p
radian	rad
second	s or sec
Siemens (voltage gain/resistance)	S
Volt (voltage)	V
Watt (power)	W

Appendix B Virtual Breadboard

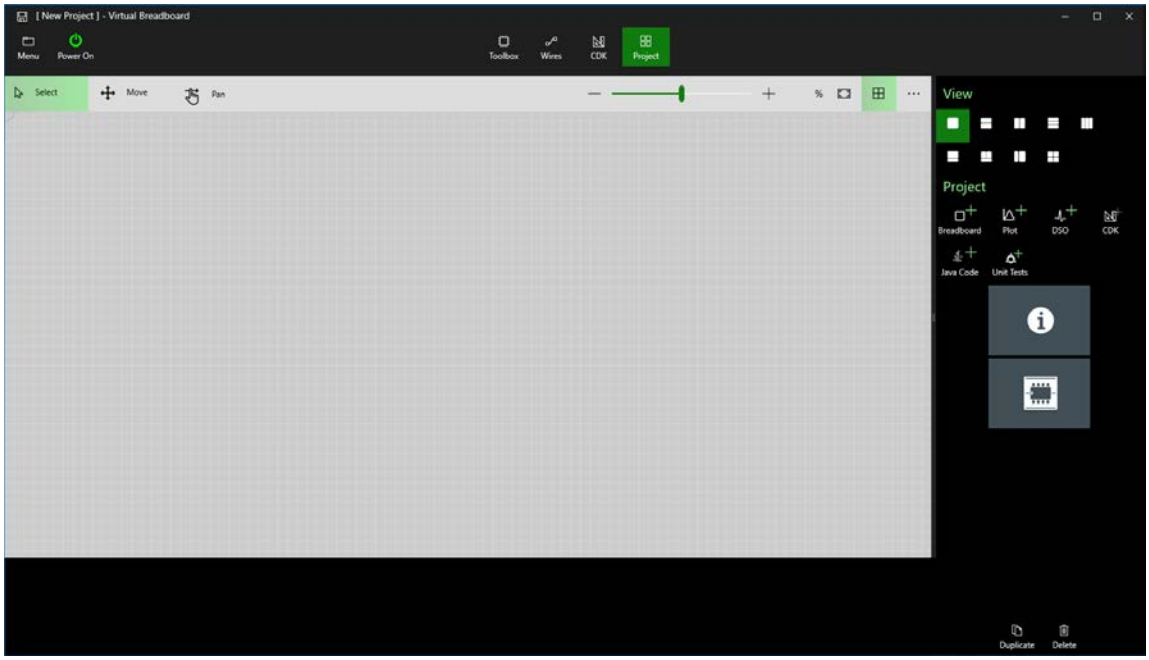
One can practice circuit construction by using a virtual breadboard. There are three virtual breadboard programs, Virtual Breadboard (VBB), Fritzing and Pebble. You may search online to find more information and select one program to use. They are similar in terms of laying out devices on the breadboard. However, each has its own characters. If a specific device is not found in the VBB library, you need to place a device in the library with the same number of pins. Pebble allows jumper wires only in the horizontal and vertical orientations. Fritzing is no longer free. It provides an additional feature, namely, the schematic view. Based on how the components are wired on the breadboard, Fritzing can generate the corresponding circuit diagram.

Shown below is a virtual operational amplifier circuit constructed by using Fritzing.



Components are listed in the right pane. There are resistor, capacitors, NPN and PNP transistors under “Basic;” ICs; and regulator under “Power.” To construct the operational amplifier circuit, a generic IC, i.e., the first item under IC, is dragged and place in the space above the breadboard. Right click. You can edit the number of pins and edit the label with the model number. You can then drag and place the IC on the virtual breadboard. The first pin on the lower left side of the IC is pin #1. Likewise, you can drag and place a resistor in the white space about the breadboard. Right click to change its orientation and resistance value. Drag and place the resistor in the circuit. Place the second resistor. Click and hold the left mouse button at the starting node to place a wire to another node. Use the upper red bus for the positive power supply. Use the lower red bus for the negative power supply. Use the lower blue bus as the ground. After completing the circuit, you can save the design.

The Virtual Breadboard App can also be used to practice laying out components on a breadboard. When VBB App starts, the following window appears.

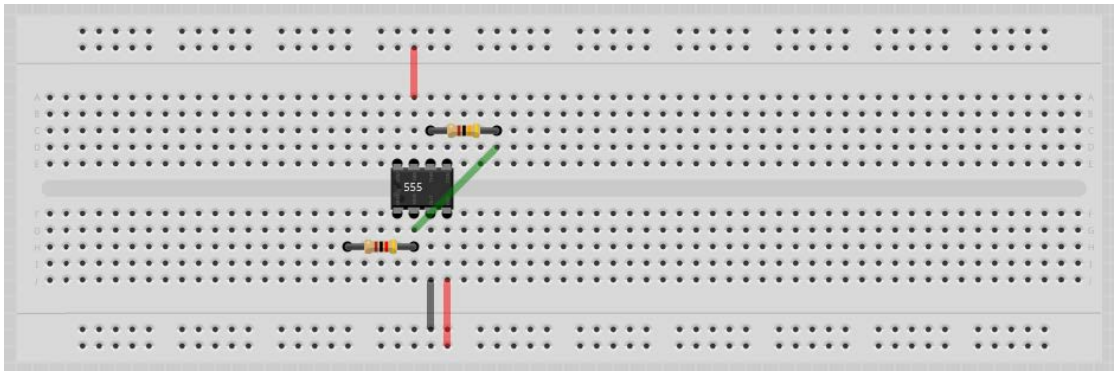


Click Toolbox. Click the second icon on the top row of tools. Click Breadboard and place it in the pane with grids. Click Toolbox to select and place components. Under the resistor icon, you can find passive components and three-pin transistors. Under the IC icon, which is the third icon in the third row, you can find a few ICs. The library of the free VBB App is very limited. For example, you can’t find the 741 operational amplifier. However, this should not prevent you from wiring the virtual circuit. You can pick 555 timer IC

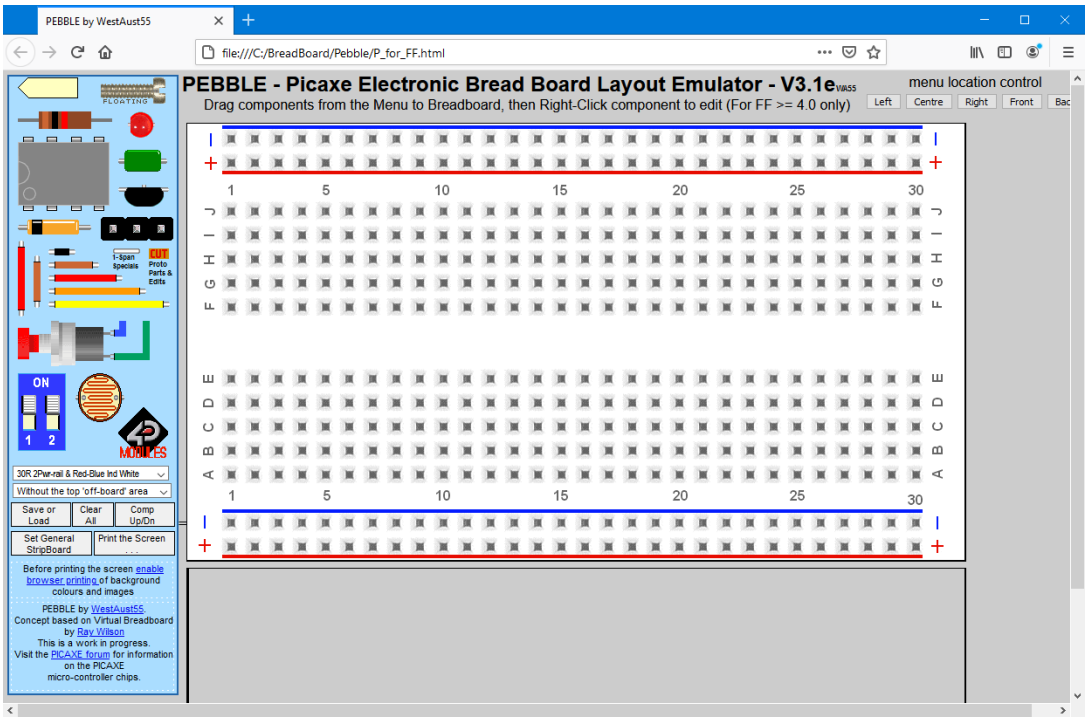
which has the same number of pins as 741. Simply wire the circuit around the IC as if it were 741. Click the resistor icon to place a resistor. Right click on the resistor to edit its resistance. Click Wires to find jumper wires. Select the color of the wire. The default wire weight of 3 pt is fine. Click the starting node. Click the ending node. Right click to terminate the jumper wire. Click Select to get out of the wiring mode.

If you want to make adjustment to an item, click Select, then, the item. You can delete, rotate, copy, and paste it. To move an item, click Move. Click and hold the left mouse button. Drag the item to a new location. To get rid of highlight, click Select. Move the mouse outside of the breadboard and press the left mouse button.

Shown below is the operational amplifier circuit constructed by VBB App. Other than an incorrect part number, it is a correctly wired operational amplifier circuit.

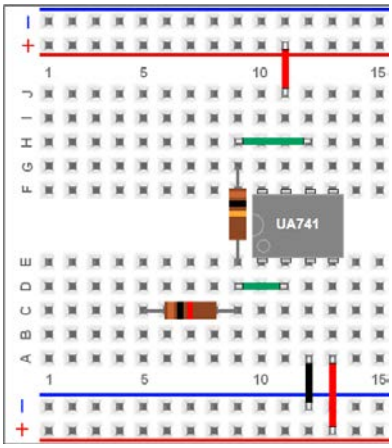


Pebble is also a virtual breadboard program. Use a browser to start Pebble. Pick a breadboard. By selecting “30R 2Pwr-rail & Red-Blue Ind White” board, the following window appears.



You can pick and drag a component to place it on the board. You can edit the pin count and part number of a semiconductor device by right clicking on it. Likewise, you can edit the resistance of a resistor and the capacitance of a capacitor. You can choose the length and color of a jumper wire.

Shown below is the operational amplifier circuit constructed by Pebble.

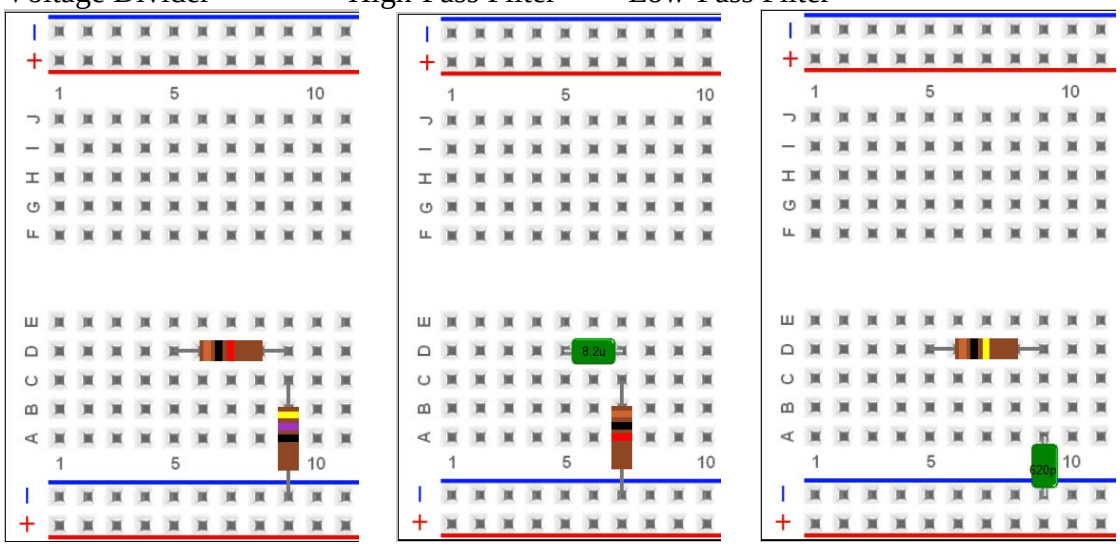


In Pebble, jumper wires must be either horizontal or vertical. Once in a while, you will find that you need several jumper wires to complete one connection.

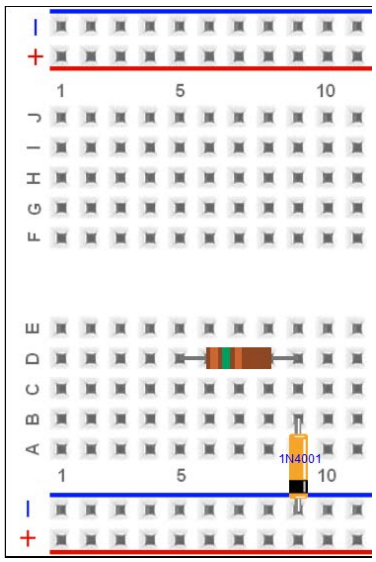
The virtual circuit can easily be viewed and verified. After confirmation, you can simply wire the real circuit on a prototype circuit board in exactly the same manner. You can also make minor changes to simplify the circuit. If you still can't get the expected waveform, there are other issues. For example, one pin of the IC is bent, hence, not properly seated on the board. The jumper wire at the banana receptacle is not in metal-to-metal contact. You will have to use the oscilloscope probe to trace the dc voltage as well as the ac signal to identify the culprit. Diagnosis can be very time consuming. It is better to be very careful in constructing the circuit than to find a trivial mistake during diagnosis. An example is to accidentally bend a pin of the IC when you place it on the board. The bent pin is pressed under the IC. You can't easily see it. The circuit won't work until you figure out what has gone wrong.

It is important to gain hands-on experiences in constructing circuits from diagrams. To help students new to circuit constrution, following examples are provided. Colored bus lines are reserved for making multiple connections, such as, power supply and ground.
Bus Line Assignments: Upper red +voltage; lower blue GND; lower Red –voltage

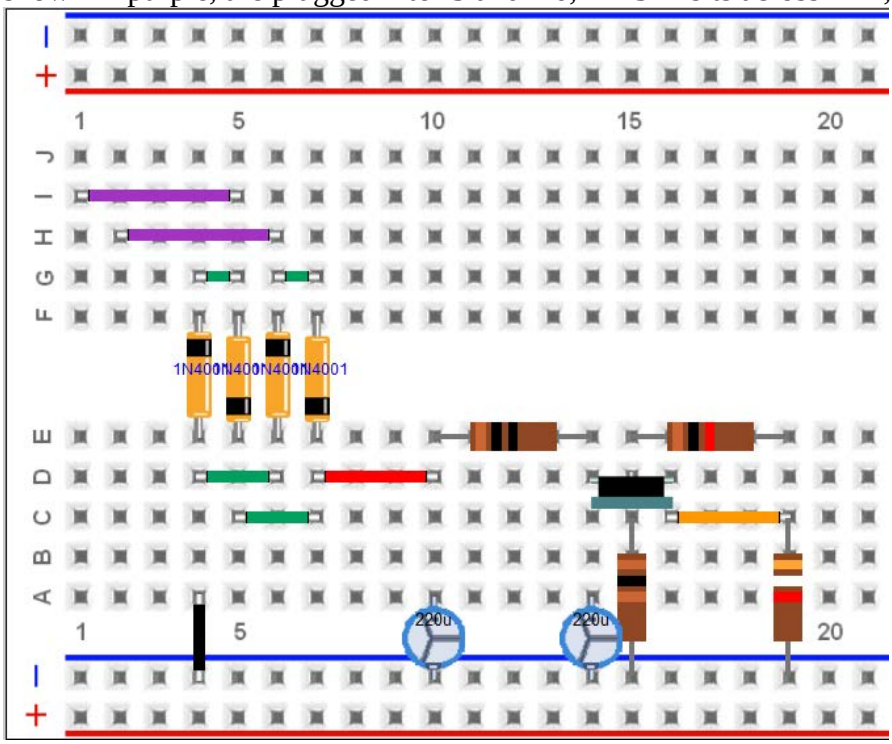
Voltage Divider High-Pass Filter Low-Pass Filter



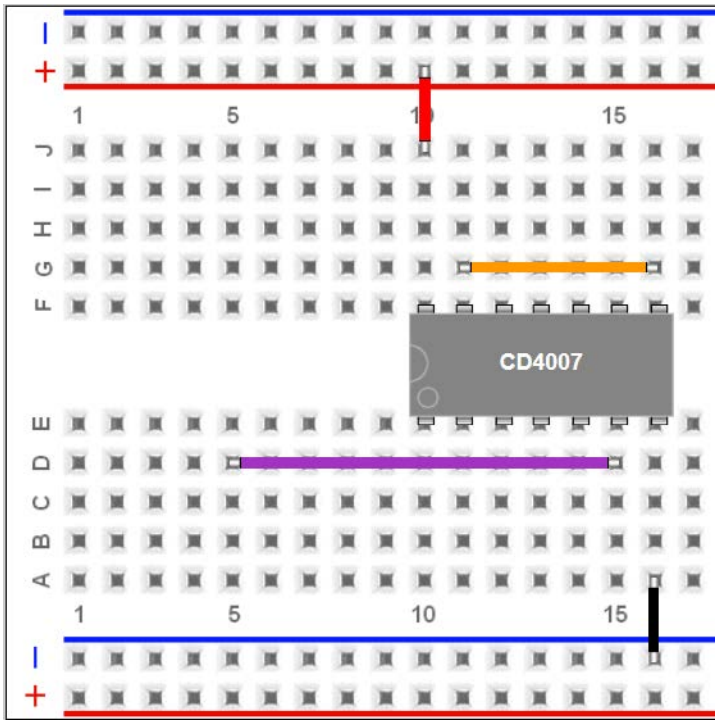
Diode Characterization



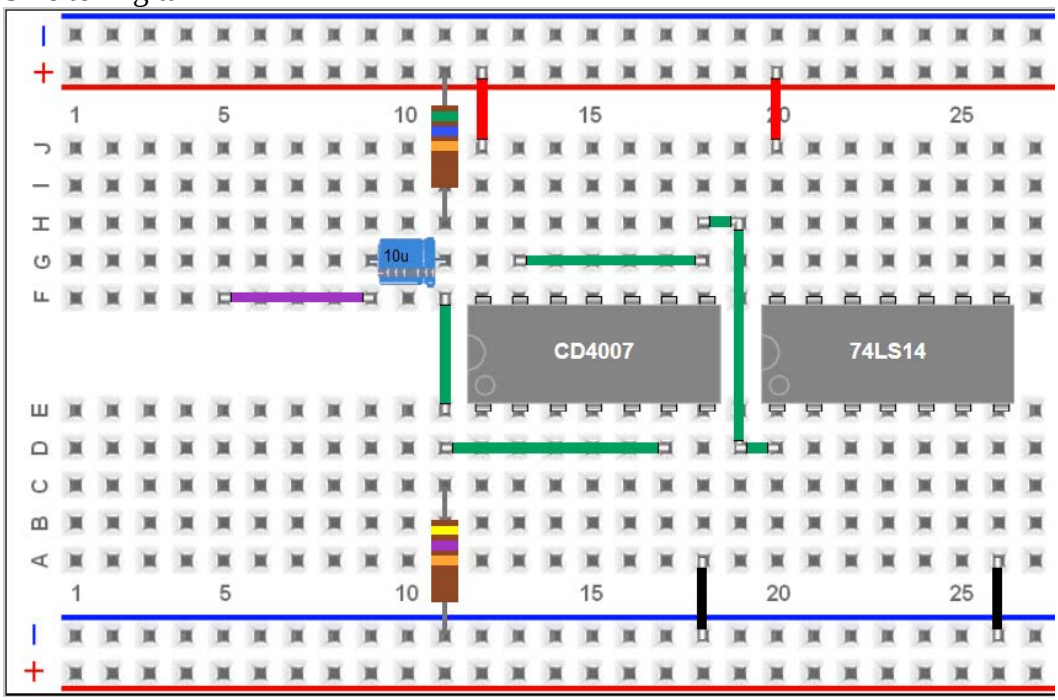
Regulated Power Supply – Transformer Without Center Tap. Two wires from transformer, shown in purple, are plugged into I5 and H6; LM317 sits across D14, D15 and D16.



CMOS Inverter

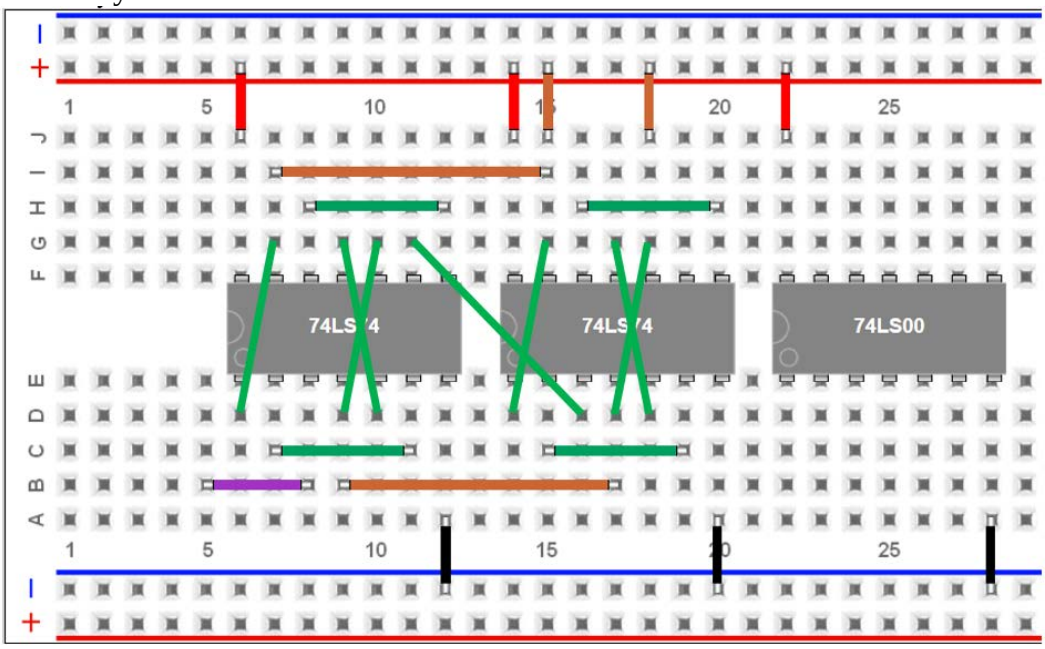


Sine to Digital



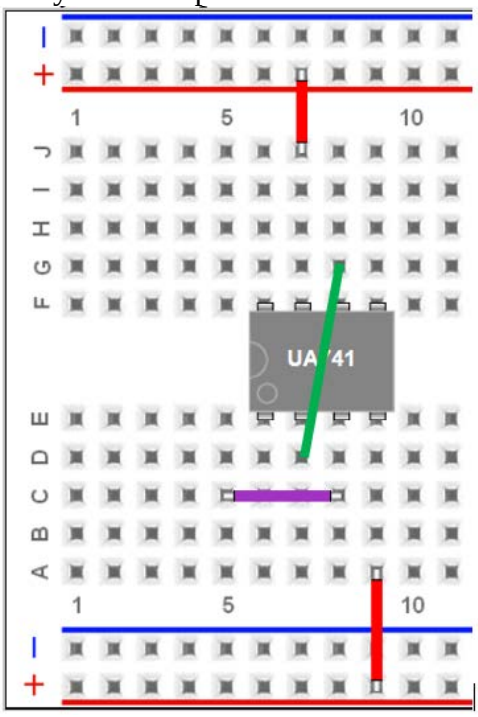
Although shown in three segments, it should be just one jumper wire from H18 to D20.

Divide-by-16

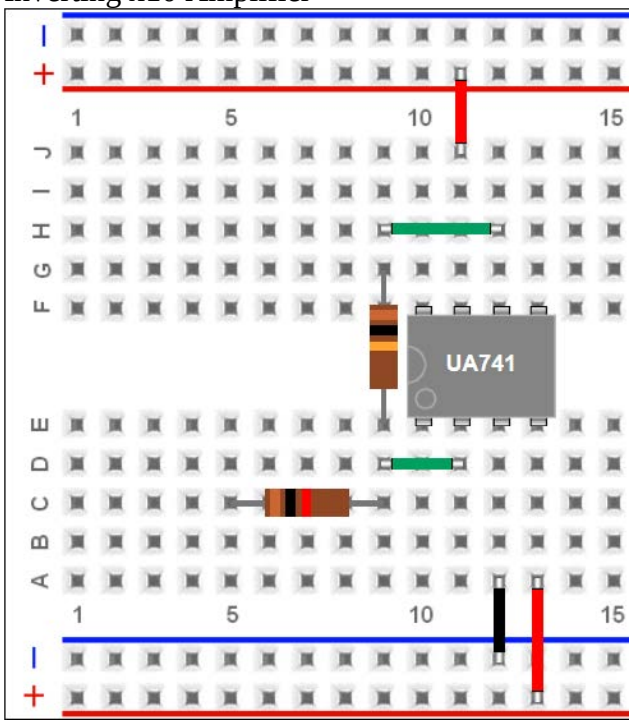


For the decade counter, reroute the jumper at J18. It should be from J18 to D24. Add two more jumper wires, between G12 and D22; between G20 and D23.

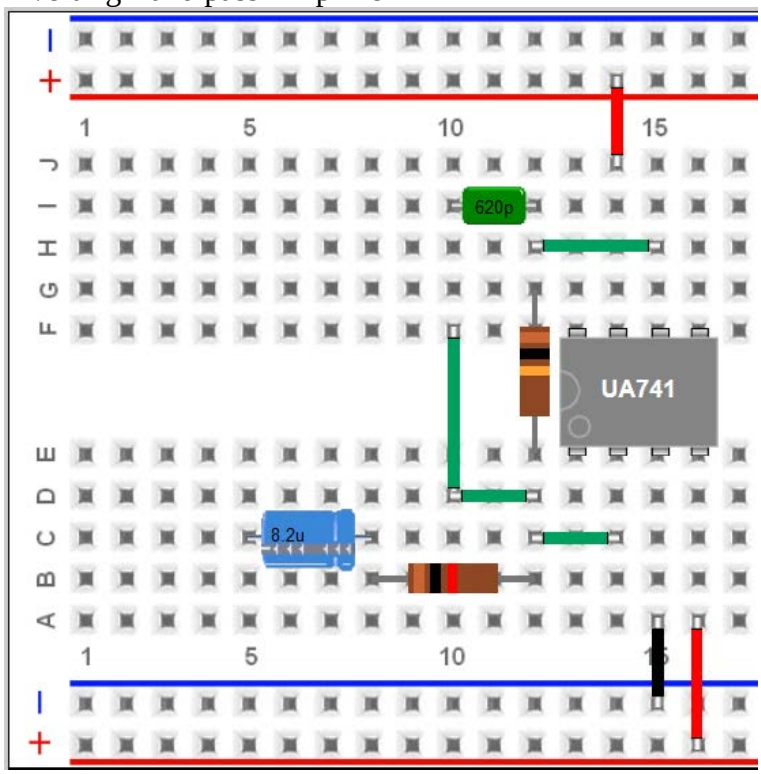
Unity Gain Amplifier



Inverting x10 Amplifier

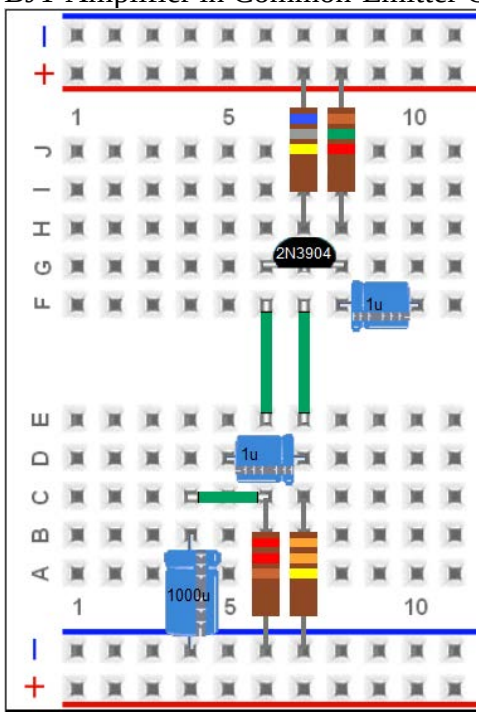


Inverting Band pass Amplifier



Although shown in two segments, it should be just one jumper wire from F10 to D12.

BJT Amplifier in Common-Emitter Configuration



Appendix C Personal Instrument Module

Most circuits discussed in the manuscript can be implemented on a prototype circuit board. To characterize circuits, one needs instruments. Developments of ICs for signal processing have made personal instrument modules readily available. They are functionally equivalent to the combination of an oscilloscope, a function generator and a power supply . Currently, there are several choices. Digilent, Inc. offers Analog Discovery 2. Analog Devices, Inc offers ADALM2000. You can pick one as your personal instrument module. There are tutorials of Analog Discovery 2 on YouTube. Digilent also provides documentations for Analog Discovery 2. Analog Devices, Inc. maintains a wiki for ADALM2000. Please follow the tutorial or wiki to get your personal instrument up and running. This appendix focuses on how to use the personal instrument module to characterize circuits.

I. Wiring

Both modules are similarly wired. A USB cable connects the micro-USB port of the module to a computer. Please be aware that the micro-USB port can be fragile. You should keep the cable connected to the module all the time. Only disconnect the cable from the computer end. The module has a block connector. According to the Digilent documentation, the connector has the following pin configuration:

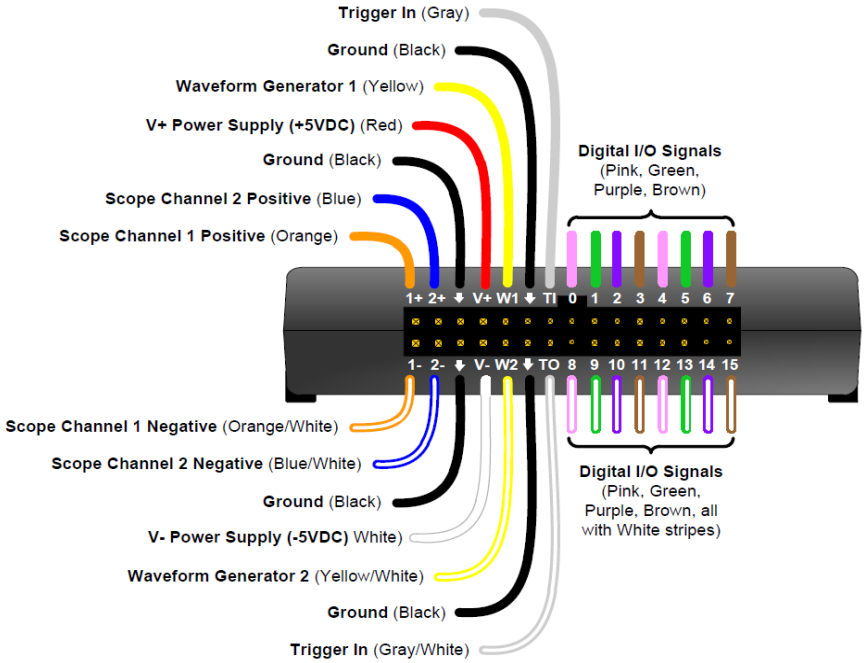


Fig. 1. The block connector of Analog Discovery 2 and its pin configuration.

If you have never used a prototype circuit board before, please find and watch a tutorial for “breadboard” on YouTube. There are bus lines, marked with red and blue, on the breadboard. You should reserve bus lines for dc power and ground connections. Some of the boards partition the bus line into blocks. The left block and the right block may be independent, i.e., not internally connected.

To connect the personal instrument module to the circuit board, you can use headers. An example is shown in the following figure. The header pin located at B3 is connected via a brown jumper wire to the positive power supply bus on the right. Likewise, the B4 pin is connected to the negative power supply bus on the left. Pin B5 is the output of the arbitrary waveform generator, W_1. It is connected to I3 which is the 1+ input of oscilloscope channel #1 by the green jumper wire . The purple jumper wire from D5 to D12 extends the output of the waveform generator W_1 to the circuit under test. The second waveform generator, W_2, is located at B6. It is not connected at this time.

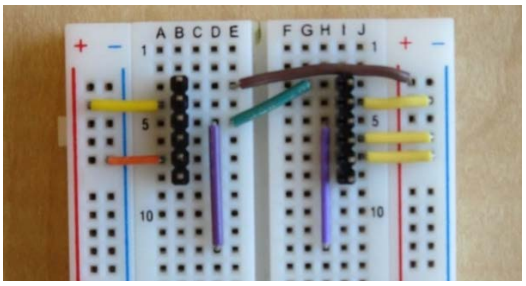


Fig. 2. The prototype circuit board with headers for connections to Analog Discovery 2.

Pin I5 is the 2+ input of oscilloscope channel #2. A purple jumper wire extends the 2+ port to H12 to facilitate connection to the circuit under test. Pins, B7, I7, are connected to the ground. You can add additional jumper wires to ground the remaining black probe wires at pins B8 and I8. There is a long jumper wire located at the far end of the prototype circuit board. It not visible in the picture. It connects two blue ground bus lines, one on the right and the other on the left, together. The oscilloscope negative input ports, I4 (1-) and I6 (2-), are connected to the ground as shown in the above picture. The oscilloscope is not operating in the differential input mode. When the oscilloscope operates in the differential input mode, they are connected to appropriate nodes in the circuit; not to the ground.

You can now attach probe wires to header pins according to the following picture: orange, orange/white, blue, blue/white, black, black; red, white, yellow, yellow/white, black, black.

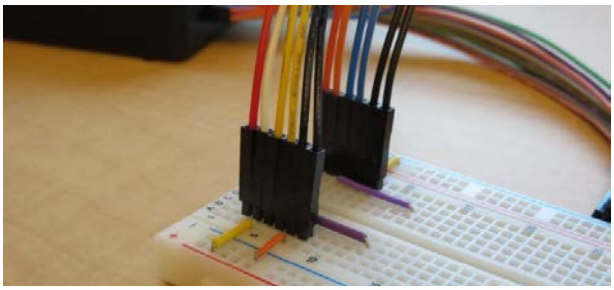


Fig. 3. The picture showing how wires from Analog Discovery 2 are connected to the board.

To characterize a low-pass filter, you can connect the instrument module to the RC circuit as shown below. The output of the waveform generator, W_1, is connected to the resistor via the lower purple jumper wire. The output of the filter is connected to oscilloscope channel #2 via the upper purple jumper wire. Oscilloscope channel #1 monitors the output of the waveform generator. Oscilloscope channel #2 monitors the output of the low-pass filter.

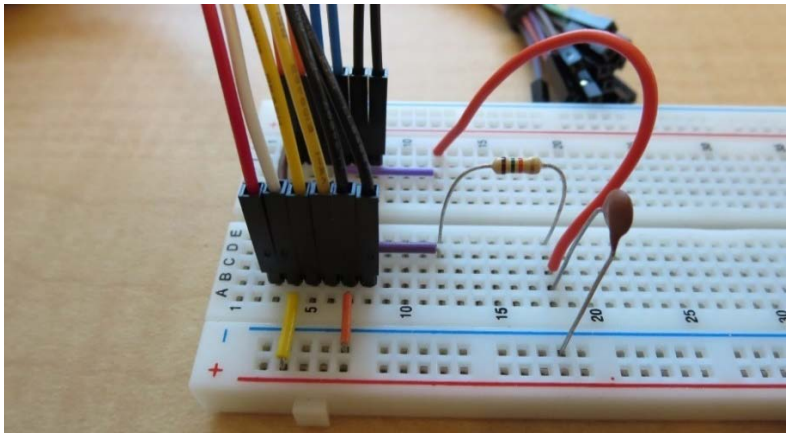


Fig. 4. A low-pass filter ready to be characterized using Analog Discovery 2.

Please note that the wiring presented above is just an example. For different circuits, you need to rewire the connections of the oscilloscope and the waveform generators, i.e., 1+, 1-, 2+, 2-, W_1 and W_2.

The dual voltage power supply of Analog Discovery 2 is limited to ±5 V and approximately 40 mA. Most circuits can and will operate properly as long as you disconnect power to circuits on the same prototype circuit board but not being tested. Once in a while you may encounter over current. This happens usually when the power supply is just turned on. When the power supply automatically shuts down due to over current,

verify circuit connections first. If there is no circuit error, reduce the filter capacitor placed between the power supply bus and the ground to 0.1 μF. During the turn-on transient, capacitors can draw a substantial amount of current.

You can combine ±5 V as a 10 V power supply for BJT amplifiers. The resistor, R_C, and the upper bias resistor are connected to +5 V. The resistor, R_E, and the lower bias resistor are connected to -5 V. Where do you connect the bypass capacitor to? You should connect the bypass capacitor to the ground. Do not connect it to -5 V. The switch mode power supply may incorporate an inductor to prevent the high-frequency switching noise from getting into the output. The concept of treating the power supply as ac ground no longer applies. In fact, the bypass capacitor in series with an inductor may cause low-frequency self-oscillation to appear unexpectedly. Please note that while using the ±5 V power supply, both the base node and the emitter node carry a negative dc voltage. The polarity of electrolytic capacitors, i.e., the emitter bypass capacitor and the input coupling capacitor, must be correctly oriented.

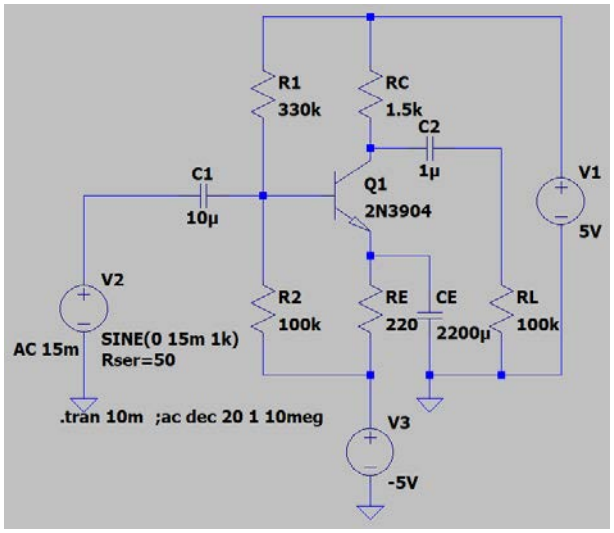


Fig. 5. The circuit diagram of a BJT amplifier powered by the dual voltage power supply.

An external power adapter can be used if the computer doesn't provide sufficient current for Analog Discovery 2 or when the circuit requires more power to operate.

High-frequency noise has been observed while using Analog Discovery 2. The dual voltage power supply in Analog Discovery 2 relies on a dc-to-dc converters to generate the negative power supply voltage. Such converter operates in the switching mode, hence, can be the source of noise. Furthermore, A/D converter operates in the multiplex mode when two or more signals are digitized. This could lead to transient switching spikes. When the

arbitrary waveform generator in Analog Discovery 2 is set to generate 1 kHz, 50 mV peak-to-peak, sinusoidal signal, there is a high-frequency noise riding on top of the sinusoidal signal. To avoid the noise, you should set the amplitude to 1 V and use a 20:1 voltage divider to attenuate the signal to the desired voltage level.

The probes of Analog Discovery 2 are very close to one another. While using Analog Discovery 2 to characterize a BJT amplifier with high gain, self-oscillation may appear. It can be eliminated by connecting a 100 pF to 1 nF capacitor at the output of the arbitrary waveform generator to the ground.

II. Characterizations of Circuits with Passive Components

In this section, circuits discussed in Chapter 3 are characterized by using Analog Discovery 2. Let's start with the voltage divider circuit shown below.

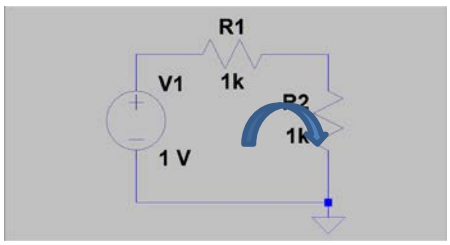


Fig. 1. The circuit diagram of a voltage divider.

The following picture shows wire connections. Wavegen 1 is the voltage source. A yellow jumper wire connects its output to the divider circuit. To measure the voltage across R_1, connect scope 1+ to the left node of R_1, i.e., the input of the divider, and scope 1- to the right node of R_1, i.e., the output node. Scope 1 measures the voltage drop across R_1. Please note that you can't make the same connection using a regular oscilloscope. Regular oscilloscopes have the negative side of the probe connected to the ground. Here, we are using the differential input mode of Analog Discovery 2. The voltage across R_2 is simply the difference of the voltage of waveform generator and the voltage across R_1.

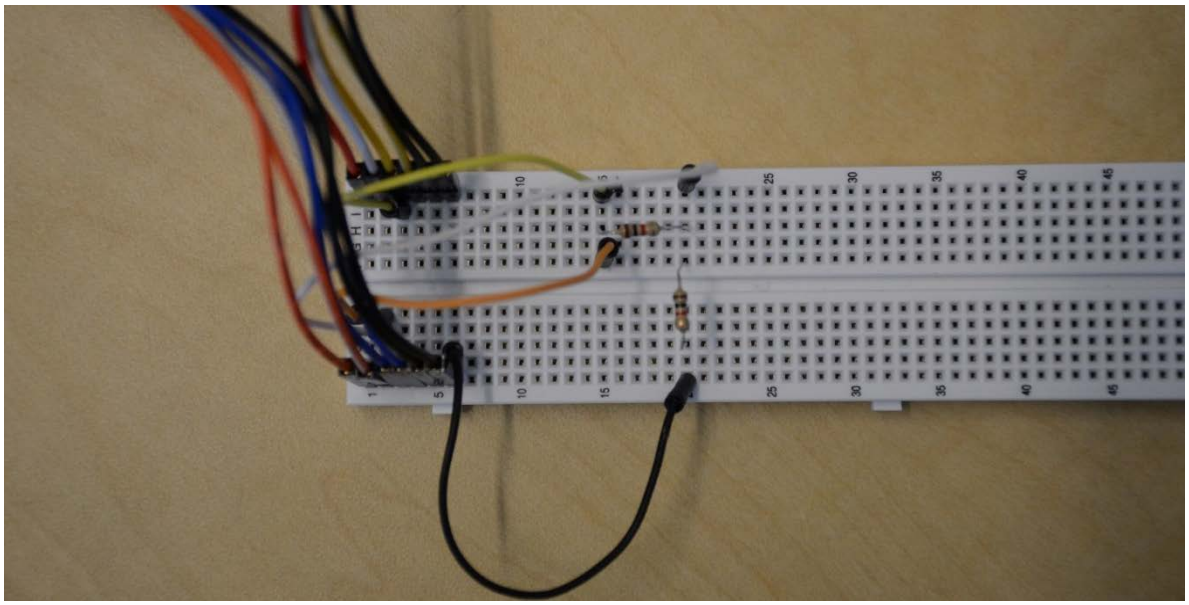


Fig. 2. The wiring of the voltage divider circuit on a prototype circuit board.

Run Wavegen channel 1 with dc and 1 V as shown in the following picture.

Fig. 3. The setup of the input signal.

Run meter as shown in the following picture.

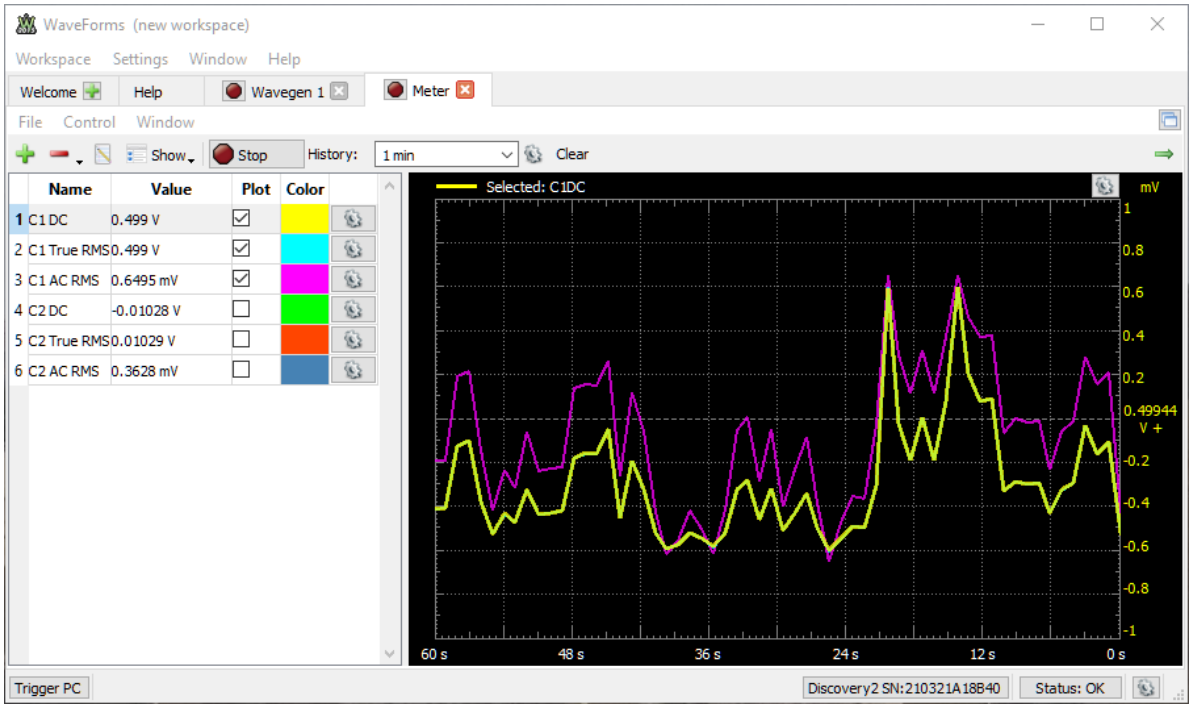


Fig. 4. The meter window displaying measured results. Only items checked are displayed.

The name, C1 dc, presents the value of the measured dc voltage across R_1. Likewise, you may also measure the voltage across R_2. Connect scope 2+ to the upper node of R_2 and scope 2- to the lower node of R_2, which is the ground node. Check C2 dc. The sum of two measured voltages should match the voltage provided by the waveform generator. There may be a small discrepancy because of noise. The resistance values of R_1 and R_2 may be slightly different from the labelled values. There may also be a small deviation reflecting the offset of Analog Discovery 2. Offset can be reduced by calibrating Analog Discovery 2. You can confirm the Kirchhoff's voltage law within an accuracy of few mV. Please note that the meter function of the module does not directly measure the current. From dc voltage measurement, you can calculate the current by dividing the voltage with resistance.

In addition to dc voltages, meter can also measure ac root-mean-square (RMS) voltage of the signal and the true RMS voltage. In true RMS measurements, the average dc component is included in the RMS calculation. The ac RMS measurement removes the average dc component before determining the RMS voltage. The graph in the meter window is a data logger. It shows sub-mV deviations due to noise around a center value of 0.49944 V.

The second circuit to characterize is shown below.

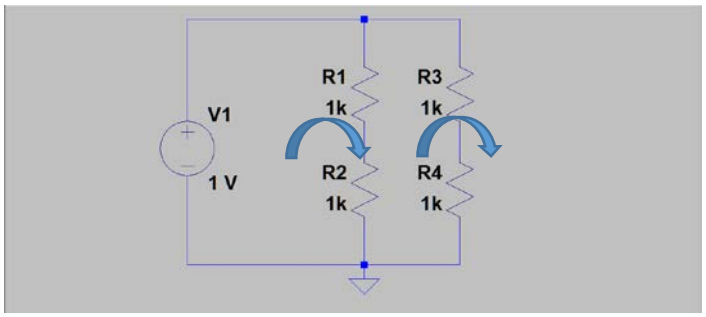


Fig. 5. The circuit diagram of the bridge circuit.

This is a Wheatstone bridge circuit. You may connect the probes and measure the voltage drop across R_1. Divide the measured voltage by the resistance to obtain the current. This is the current flowing through R_1 and R_2. Measure the voltage drop across R_3. Divide the measured voltage by the resistance to obtain the current flowing through R_3 and R_4. You will find that the current in both branches is 0.5 mA. Any small discrepancy may result from deviations of actual resistances from the values marked.

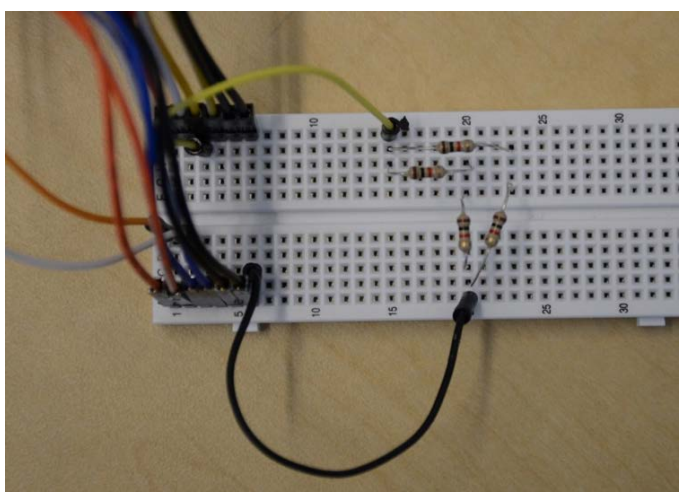


Fig. 6. The bridge circuit connected on the prototype circuit board. Only the voltage source and the ground connections are shown. Readers can practice how to connect the probes.

To characterize circuits with capacitors or inductors, we use ac signals. An ac signal is defined by its shape, amplitude and frequency. We often use sine wave and square wave to characterize circuits. The span from the positive peak to the negative peak, which is easy

to measure by using an oscilloscope, is two times the amplitude. The product of period, *T*, and frequency, *f*, is unity. A 1-kHz signal has a period of 1 msec. The time delay within each cycle is translated into a phase shift between 2π or 360^0. Divide the delay with the period to find the phase shift. The sinusoidal signal facilitates characterizations in the frequency domain. By scanning the frequency of the input sinusoidal signal, characteristics of the circuit as a function of frequency can be measured. Oscilloscope can monitor time-dependent waveforms. In the scope display, you can adjust the time base, i.e., the horizontal scale, and the vertical sensitivity or range. The color of the vertical scale is linked to the corresponding channel. Yellow color shows settings of channel 1. Offset moves the trace up and down. It is used to separate two traces when they overlap. The left yellow triangle marks the zero voltage reference for channel 1. The triangle on the right indicates the trigger level. It also corresponds to the voltage of the waveform at the center of the display. Trigger source can be channel 1 signal or channel 2 signal. Choose the stronger signal as the trigger. You can click view, data to see the digitized data. You can also copy and paste the data to a spreadsheet.

The next circuit to characterize is an *RC* filter circuit with a 1-kΩ resistor and a 0.1 μF-capacitor. The color bands on the carbon film resistor should be brown, black and red. The label on the ceramic disc capacitor should be 104. Just like the voltage divider circuit, the output node is located at the upper right-hand corner. This is a low-pass filter circuit.

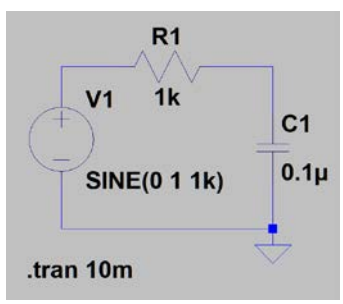


Fig. 7. The diagram of an *RC* filter circuit. The resistor is in the front. It is a low-pass filter circuit.

Here is the circuit constructed on the prototype circuit board:

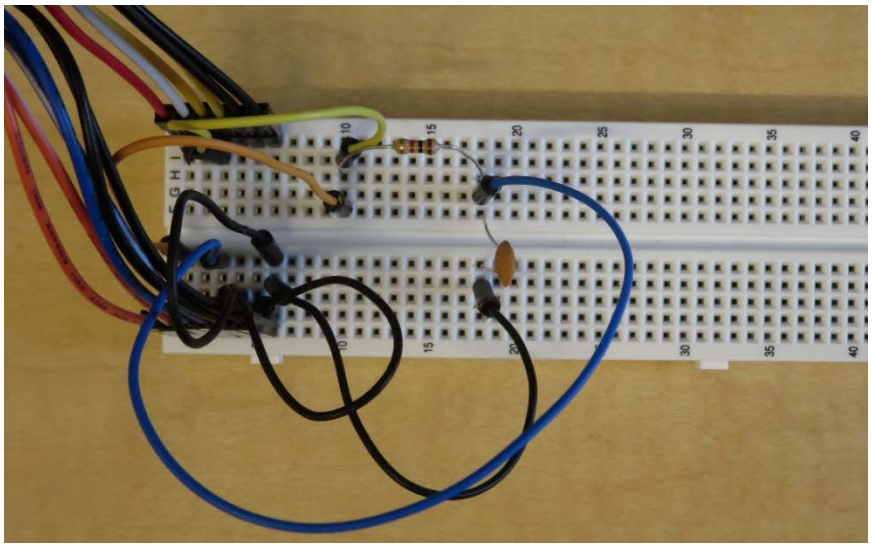


Fig. 8. The low-pass filter circuit constructed on the prototype circuit board. Jumper wires connect the input signal from the waveform generator and output signal to the oscilloscope.

Run wavegen 1 with an amplitude of 1 V and frequency of 1 kHz. Connect scope 1+ to the output of wavegen 1, 1- to the ground. Connect scope 2+ to the output node, i.e., upper node of capacitor, 2- to ground. Run scope. You will see the following waveforms:

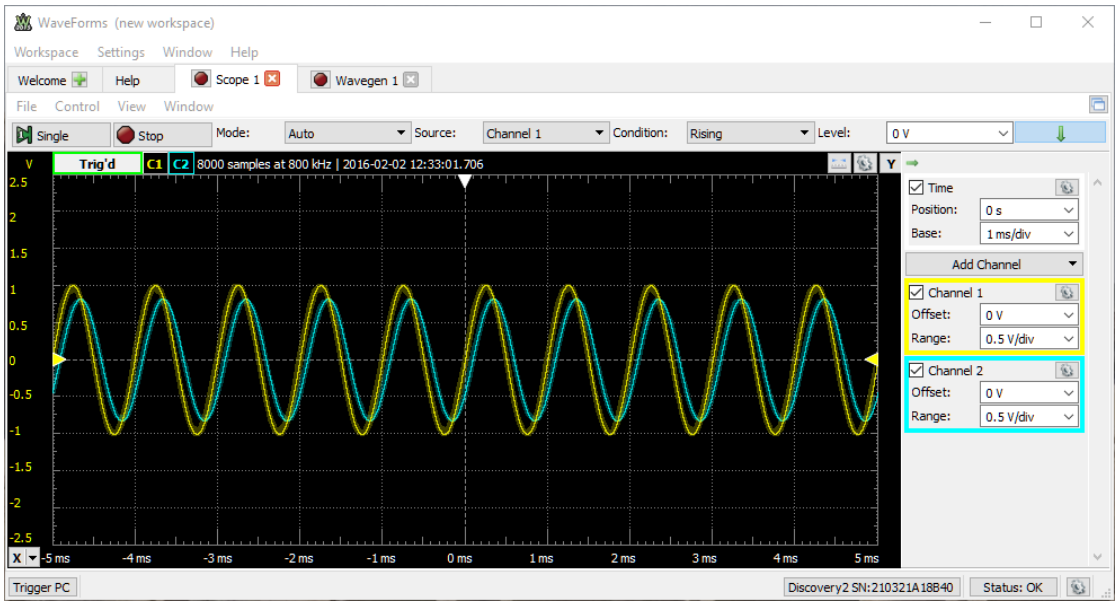


Fig. 9. The input signal shown in yellow and the output waveform shown in cyan color of the low-pass filter.

Capacitor introduces a phase delay. The peak of voltage across the capacitor reaches maximum at a later time than the peak of the sinusoidal input. According to the Kirchhoff's voltage law, the difference between these two waveforms should be the signal across the resistor. You can measure the voltage across the resistor by moving the 2+ probe to the left node of resistor and the 2- probe to the right node of the resistor.

To see the response of the circuit as a function of frequency, run network. Select the starting frequency at 100 Hz and stop frequency at 100 kHz. For signal throughput, network uses the log scale. This is the Bode plot that you will see. The amplitude decreases and the phase angle approaches asymptotically to -90^0 as the frequency increases. Low-frequency signal passes through without attenuation while the high-frequency signal is attenuated. The horizontal frequency axis is in the $\log_{10}$ scale to cover multiple orders of magnitude.

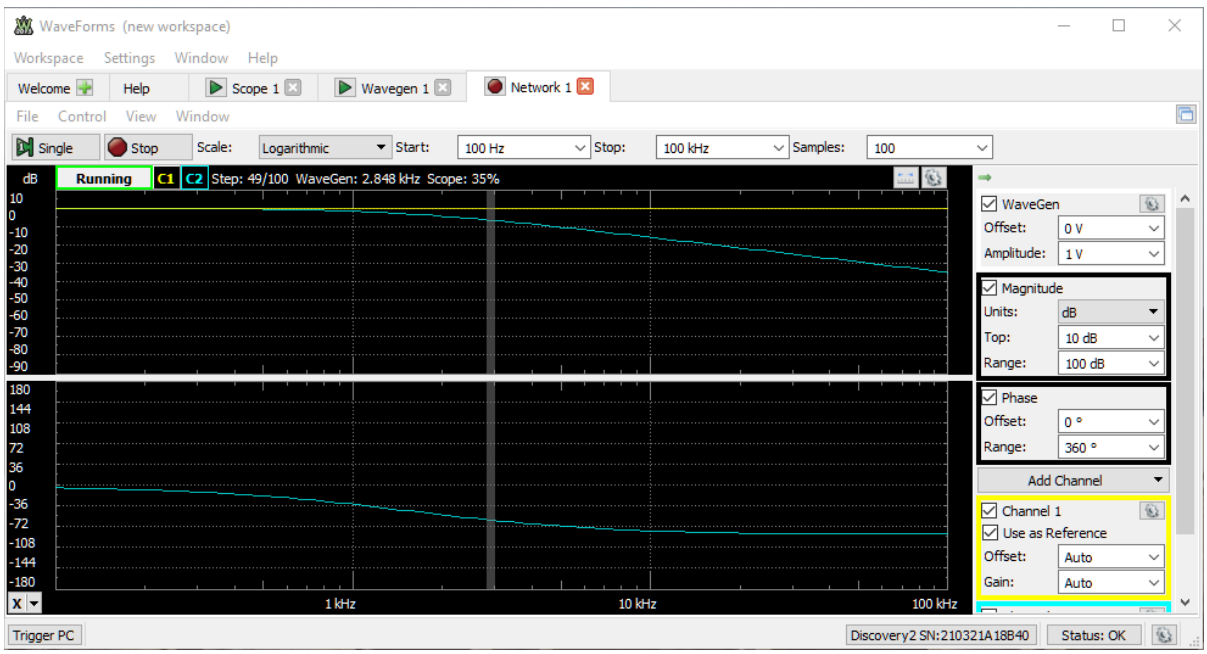


Fig. 10. The Bode plot showing the power throughput and phase of the low-pass filter as a function of frequency.

The square wave or clock signal is also used in characterizing circuits, especially, digital circuits. The response of the *RC* circuit to a positive step voltage, which occurs at the rising edge of the square wave, can be determined by solving the first-order differential equation. You can observe such a waveform by monitoring the voltage across the capacitor. Change wavegen 1 to square wave, 100 Hz. The amplitude remains at 1 V. In the scope

window, you can find the voltage across the capacitor shown in blue. The yellow trace is the step input voltage.

Fig. 11. The input and output waveforms of the low-pass filter. The yellow trace is the input step voltage. The waveform shown in cyan color is the voltage across the capacitor.

The capacitor integrates the current to generate the output voltage. Therefore, a low pass filter is an integrator. The main application of the low-pass filter is to suppress the high-frequency noise.

By exchanging locations of resistor and capacitor in the circuit, we obtain a high-pass filter. The input signal is connected to the capacitor and the output is across the resistor. Under the same driving conditions or settings of wavegen 1, waveforms of the high-pass filter are shown below for sine wave and square-wave excitations, respectively.

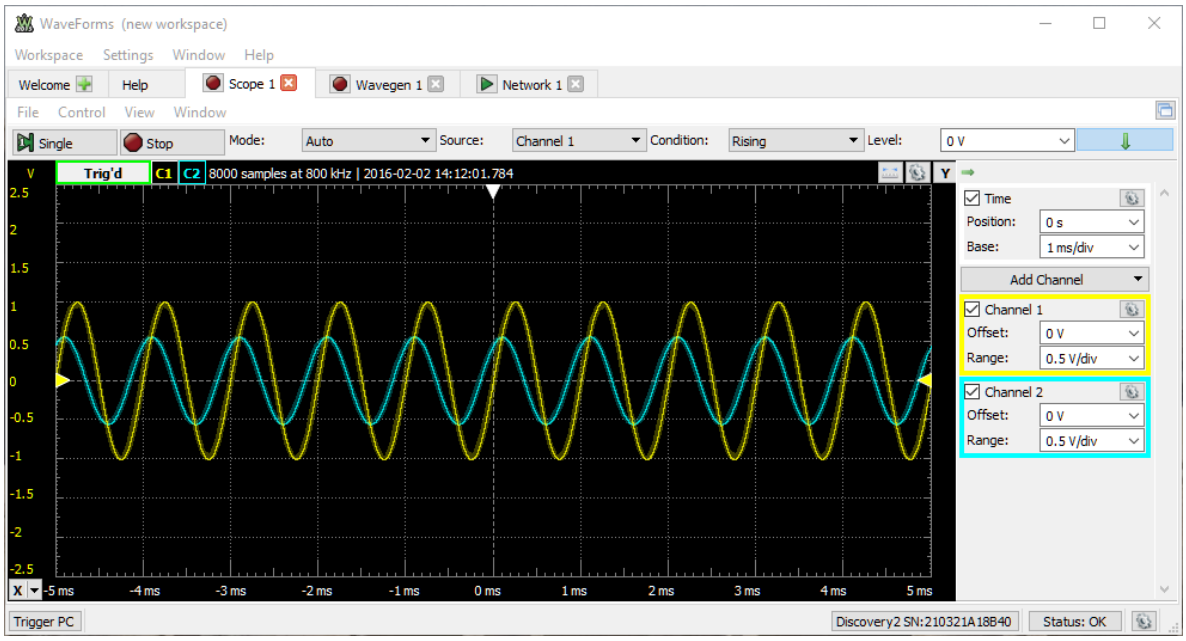


Fig. 12. The input and output waveforms of the high-pass filter. The input is shown in yellow and output in cyan color.

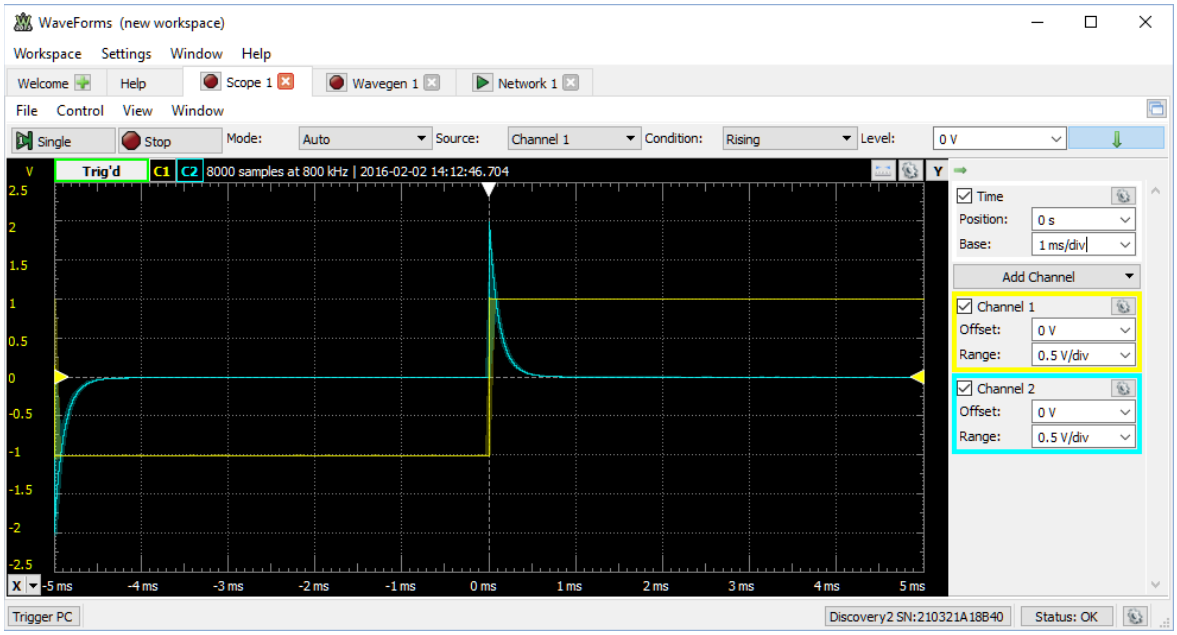


Fig. 13. The response of a high-pass filter. The yellow trace is the input step voltage. The waveform shown in cyan color is the voltage across the resistor.

With sinusoidal signal, the frequency response is shown in the following Bode plot:

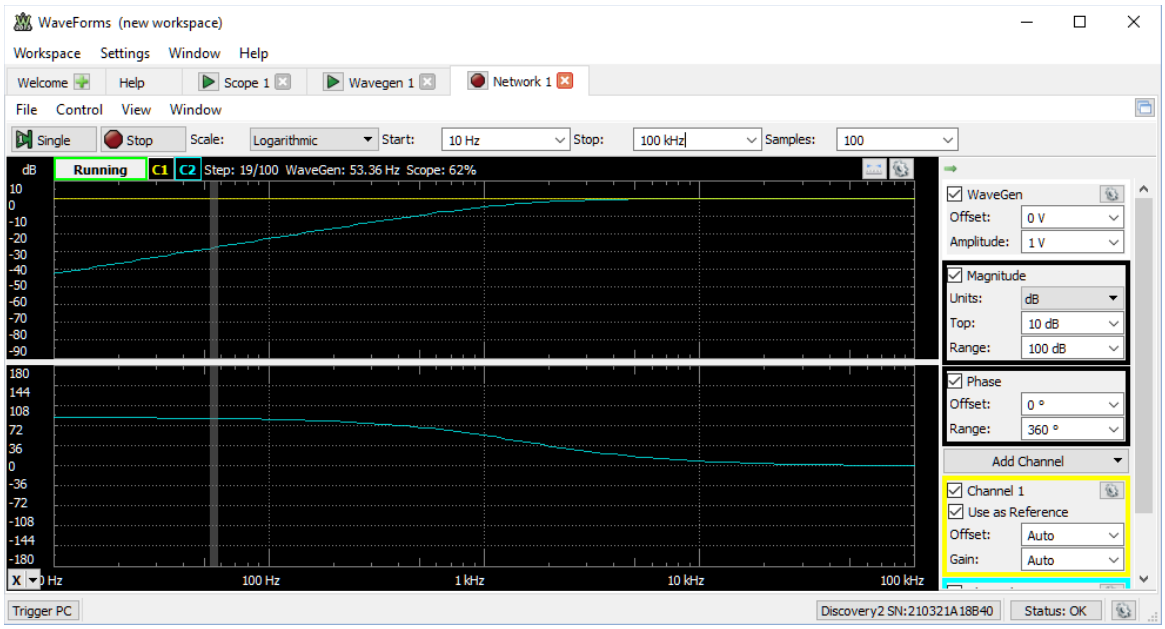


Fig. 14. The Bode plot showing the power throughput and phase of the high-pass filter as a function of frequency.

The next circuit to analyze is the *RLC* circuit. There are two configurations, one with *LC* in series and the other in parallel. Shown below is the circuit with *LC* in series.

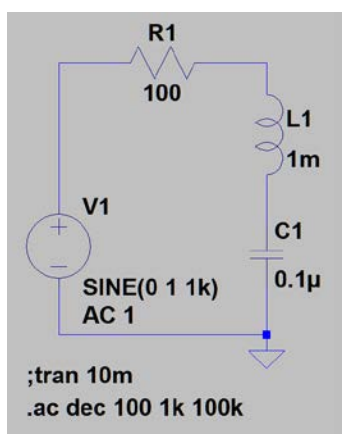


Fig. 15. The diagram of the series *RLC* circuit.

The circuit constructed on the prototype circuit board using components in the analog parts kit, 100 Ω resistor, 100 nF capacitor, and 1 mH inductor, is shown below.

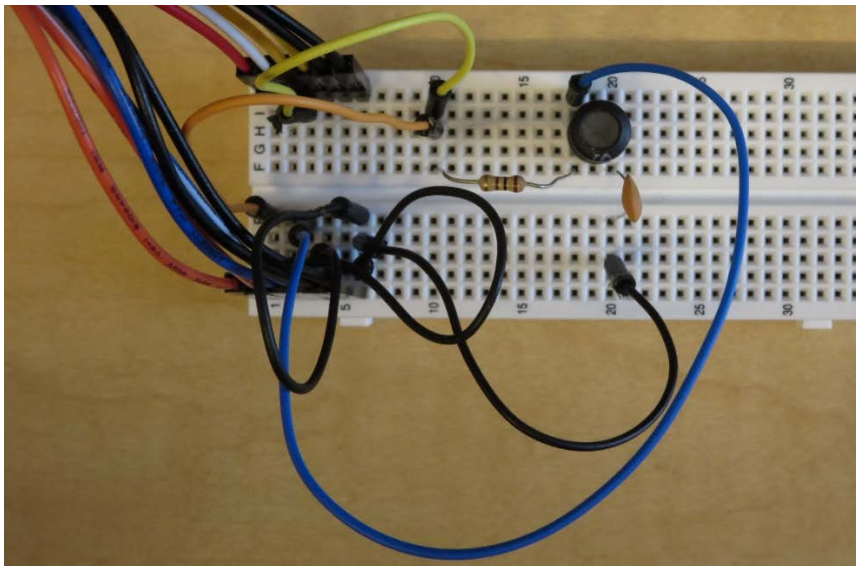


Fig. 16. The series *RLC* circuit constructed on the prototype circuit board. Jumper wires connect the input signal from the waveform generator and the output signal to the oscilloscope.

Shown below is the Bode plot obtained by performing the network analysis. The resonance frequency is at 15.9 kHz. The output is -20 dB below the input.

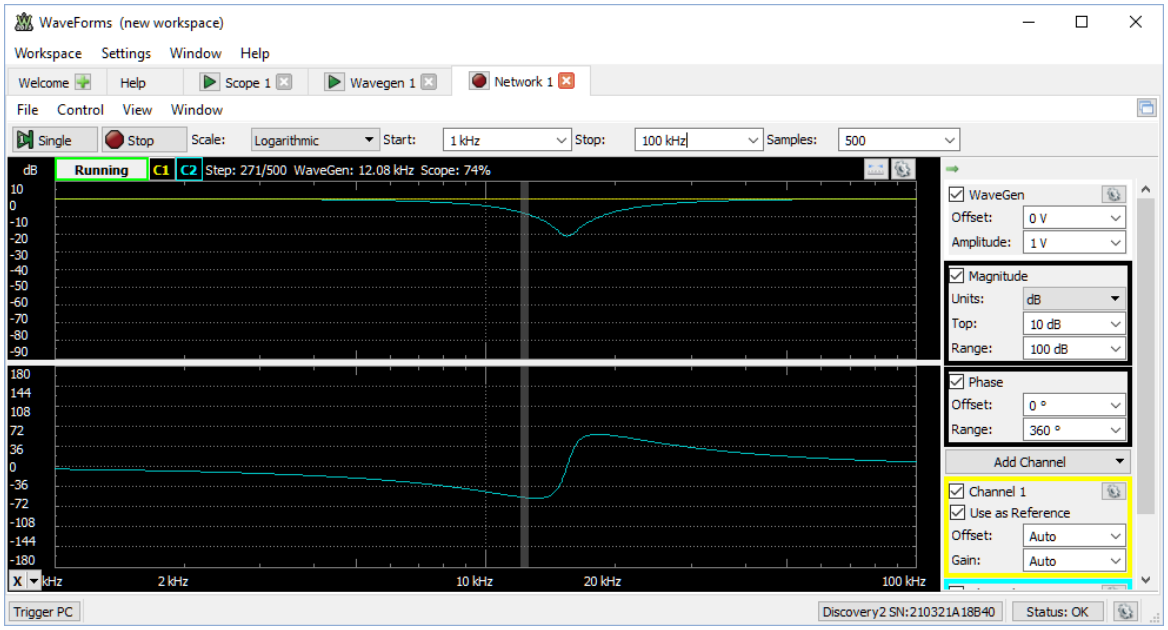


Fig. 17. The Bode plot showing the power throughput and phase of the series *RLC* circuit as a function of frequency.

Show below is the measured voltage across the 100-Ω resistor as a function of time. The current is given by voltage divided by resistance. The input square wave is shown in yellow. The voltage across the resistor is presented in cyan color.

Fig. 18. The response of a series *RLC* circuit. The yellow trace is the input step voltage. The waveform shown in cyan color is the voltage across the resistor.

Similarly, we can construct an *RLC* circuit with inductor and capacitor in parallel.

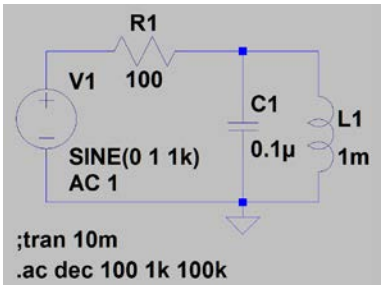


Fig. 19. The diagram of the *RLC* circuit with *L* and *C* in parallel.

Shown below in the measured Bode plot.

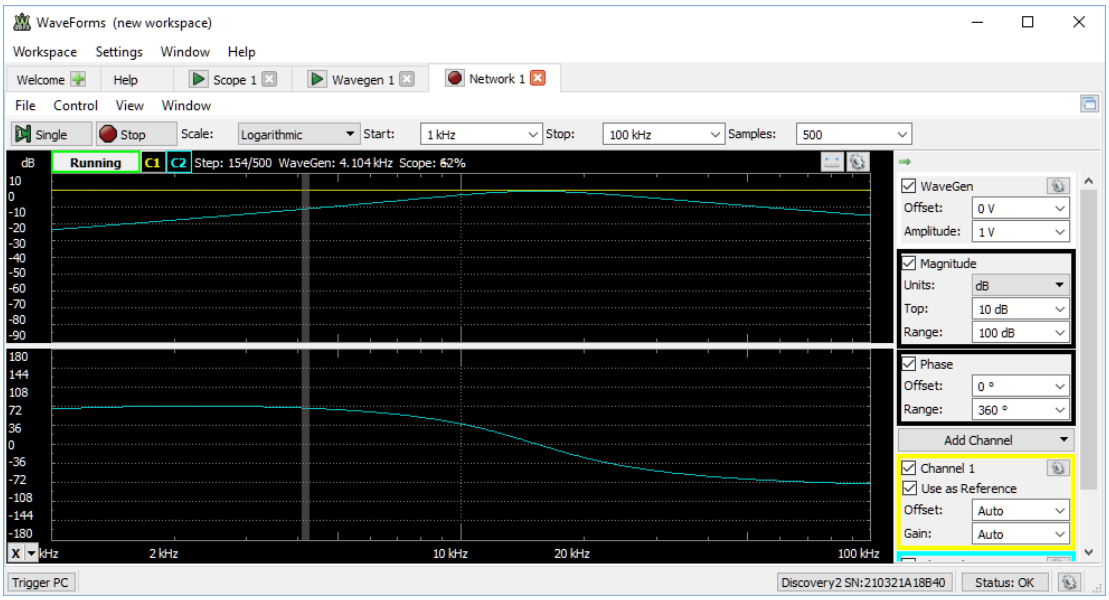


Fig. 20. The Bode plot showing the power throughput and phase of the *RLC* circuit with *L* and *C* in parallel as a function of frequency.

You can drive the circuit with a square wave and determine the current by monitoring the voltage across the resistor. The current has a transient spike followed by damped relaxation oscillation before reaching the steady state as shown below.

Fig. 21. The response of the *RLC* circuit with *L* and *C* in parallel. The yellow trace is the input step voltage. The waveform shown in cyan color is the voltage across *R*.

Waveforms and Bode plots obtained from measurements can be compared to results of simulations presented in Chapter 4. In simulations, all components are ideal. In physical circuits, inductors have a finite resistance and labeled values of components are not exact. The peak in a Bode plot can become shallow. The resonance frequency can be slightly off.

III. Characterizations of Semiconductor Devices

Construct the following diode characterization circuit on the prototype circuit board. The waveform generator W_1 scans from -5 V to 5 V. By also using the negative power supply of the instrument module set at -5 V, the extended scanning range of voltage across the diode becomes 10 V. The diode current is monitored by using oscilloscope channel #2 in the differential mode. The diode voltage is monitored by oscilloscope channel #1. As shown in the following figure, both 1+ and 2- are connected to the anode; 1- is connected to the cathode; 2+ and W_1 are connected to the left node of the resistor, R_1.

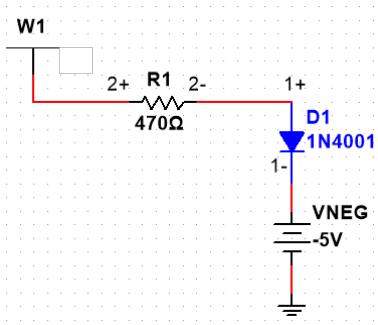


Fig. 1. The diode characterization circuit.

Set and run the waveform generator W_1 for triangular wave, 100 Hz and 5 V amplitude. Run the oscilloscope using exactly the same settings, e.g., time base, offset, range, as shown in the following picture. Click “View”, “Add XY”. The horizontal axis is the diode voltage. The vertical scale is proportional to the diode current. The diode current can be calculated from the voltage across the resistor divided by its resistance. Since a 470-Ω resistor is used, each vertical unit corresponds to 2.13 mA. Export and save the graph as well as the data.

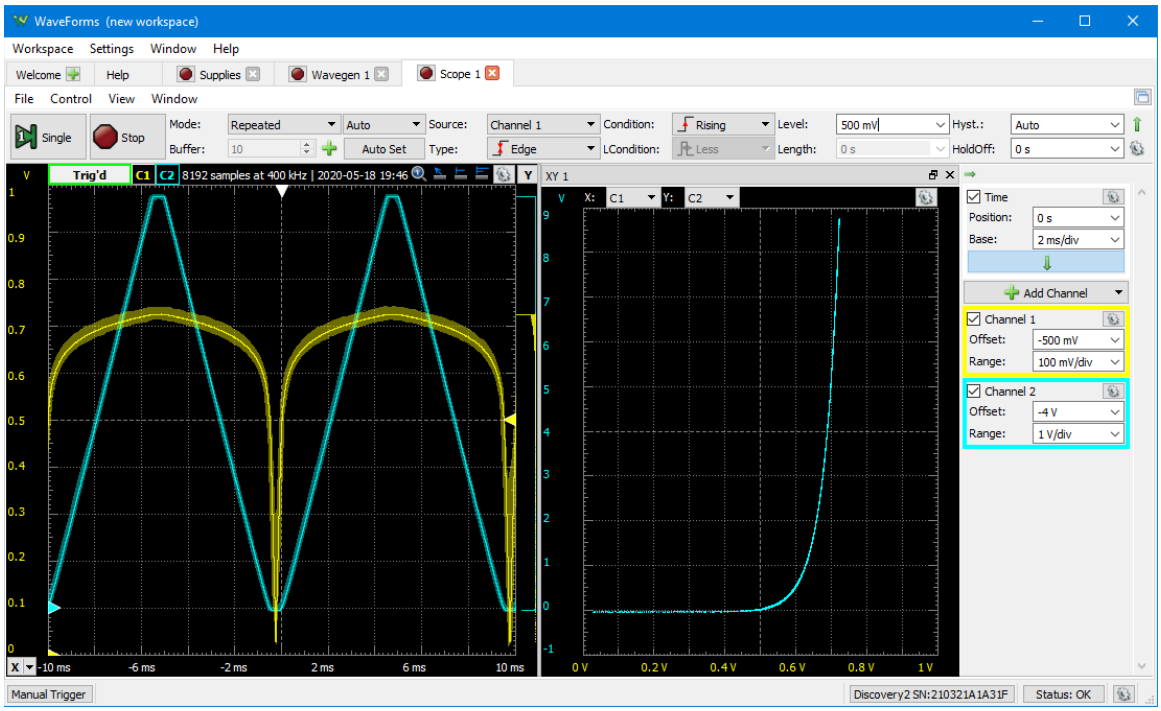


Fig.2 The I-V plot of the diode.

You can apply the same method to characterize MOSFET and BJT. To obtain the output characteristics, construct the following BJT characterization circuit on the prototype circuit board. The waveform generator W_1 scans from -5 V to 5 V. By also using the negative power supply of the instrument module set at -5 V, the extended scanning range of V_{CE} becomes 10 V. The collector current is monitored by measuring the voltage drop across the resistor using oscilloscope channel #2 in the differential mode. The collector to emitter voltage is monitored by oscilloscope channel #1. As shown in the following figure, both 1+ and 2- are connected to the collector; 1- is connected to the emitter; 2+ and W_1 are connected to the upper node of the resistor, R_C. None of the negative input probes is connected to the ground. The second waveform generator, W_2, is connected to R_1. It controls the base current.

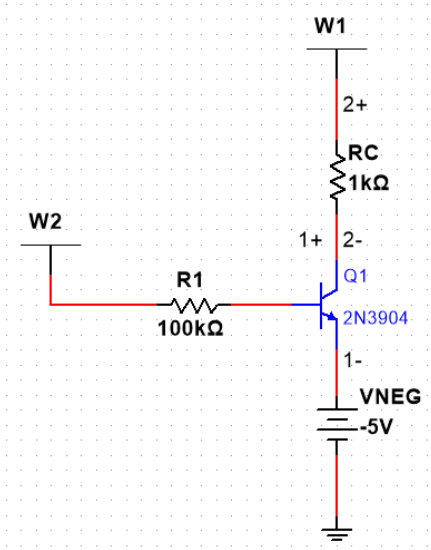


Fig. 3. The transistor characterization circuit.

We need to obtain a series of I_C versus V_{CE} curves, one for each base current. In order to obtain these curves, two waveform generators need to work in synchronism. Waveform generator #1 generates the triangular wave. There is one full triangular wave cycle during each voltage step generated by the waveform generator #2. Run Waveforms. Select "Wavegen" under "Welcome". Click "Channels" and have both channels selected. Change the setting from "Not Synchronized" to "Synchronized". Use the text editor, Notepad, to create and save a text file, ramp.txt, consisting of six lines, each line with a number as shown below.

-5
-4
-3
-2
-1
0

Set up and run both waveform generators exactly according to the following figures. Waveform generator #1 generates a triangular wave. Please note how the frequency, amplitude, and phase are set. Use exactly the same values.

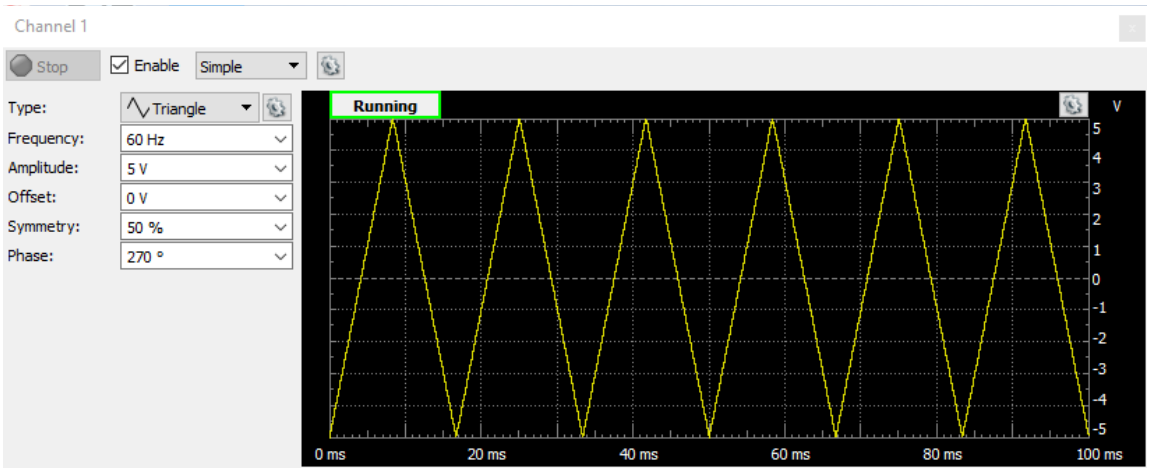


Fig. 4. The settings of the waveform generator #1.

Run the waveform generator #2 in the custom mode. Import the text file. Set the frequency, sampling rate according to the figure below.

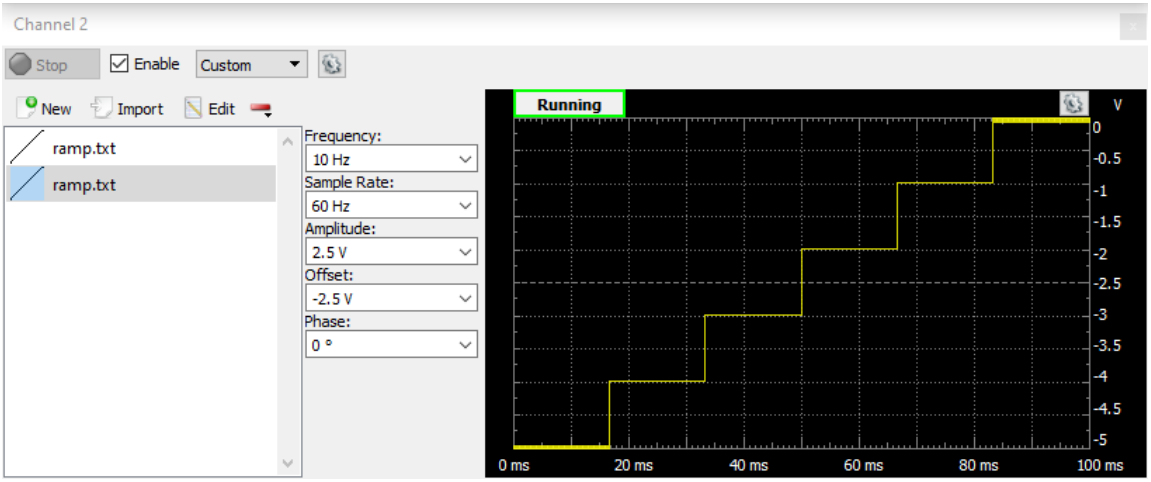


Fig. 5. The settings of the waveform generator #2.

During each step, the triangular wave completes one cycle. Since the frequency of the triangular wave is 60 Hz and there are six steps, the frequency of the step waveform should be 10 Hz. The two waveform generators are synchronized. Together, they generate the curves in the plot.

Run the negative dc power supply at -5 V. Run the oscilloscope using exactly the same settings, e.g., time base, offset, range, as shown in the following figure. Click “View”, “Add XY”.

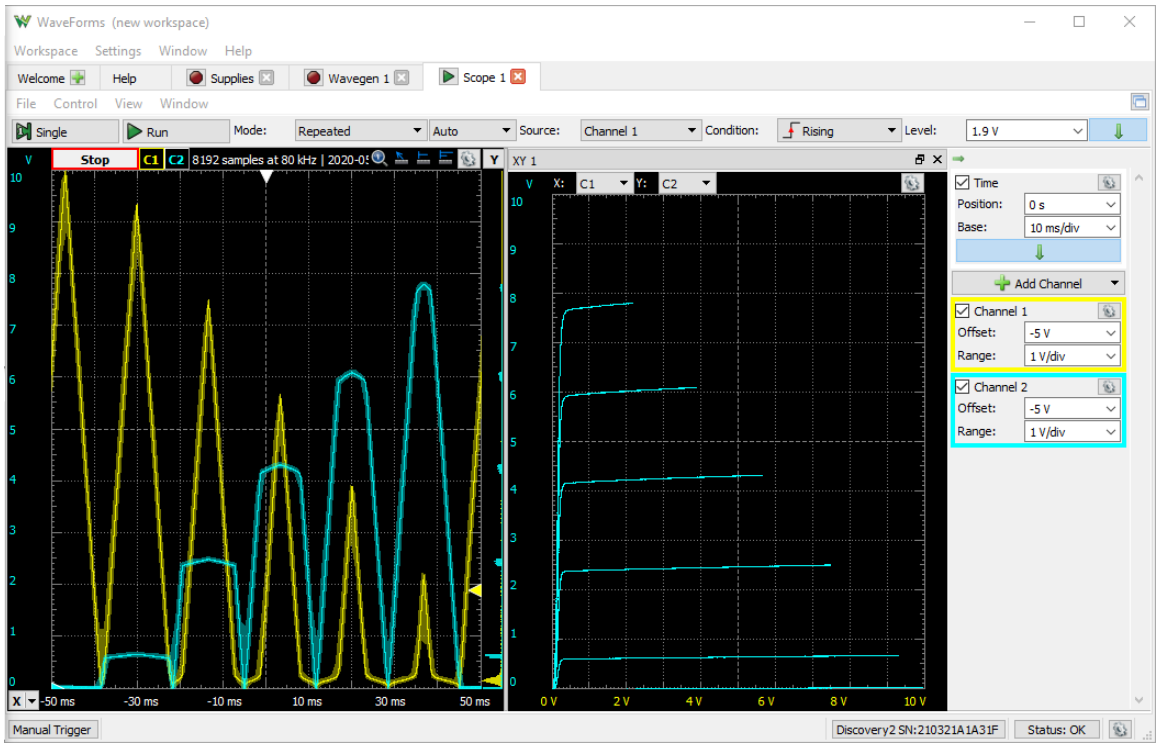


Fig. 6. The I_C versus V_{CE} characteristics of a transistor.

The plot on the right-hand side is the transistor output characteristics. The horizontal axis is V_{CE}. The vertical scale corresponds to I_C in mA because a 1-kΩ resistor is used in the circuit. Click "File", "Export" to save the plot; then, data as a text file which can be read by Excel. There are six curves in the plot. From bottom to top, they correspond to approximately a base current of 0 µA, 3.2 µA, 13.1 µA, 23 µA, 32.5 µA, and 42 µA, respectively.

For the input characteristics, there is also a series of curves, one for each V_{CE}. Revise the circuit as shown below.

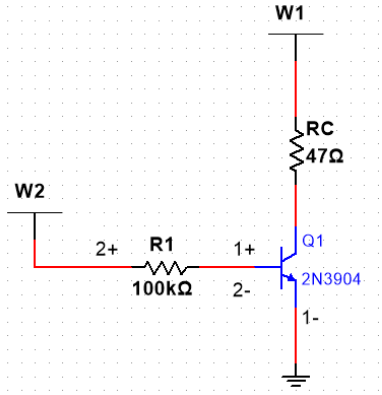


Fig. 7. The transistor input characterization circuit.

Set up two waveform generators according to the following figures, one for W_1 and the other for W_2. For waveform generator W1, you need to use the text editor, Notepad, to create a text file consisting of six lines, each line with a number, 5, 4, 3, 2, 1, 0. Use the custom setting and import the text file to generate the step waveform. Set the frequency so that it is synchronized to waveform generator W_2.

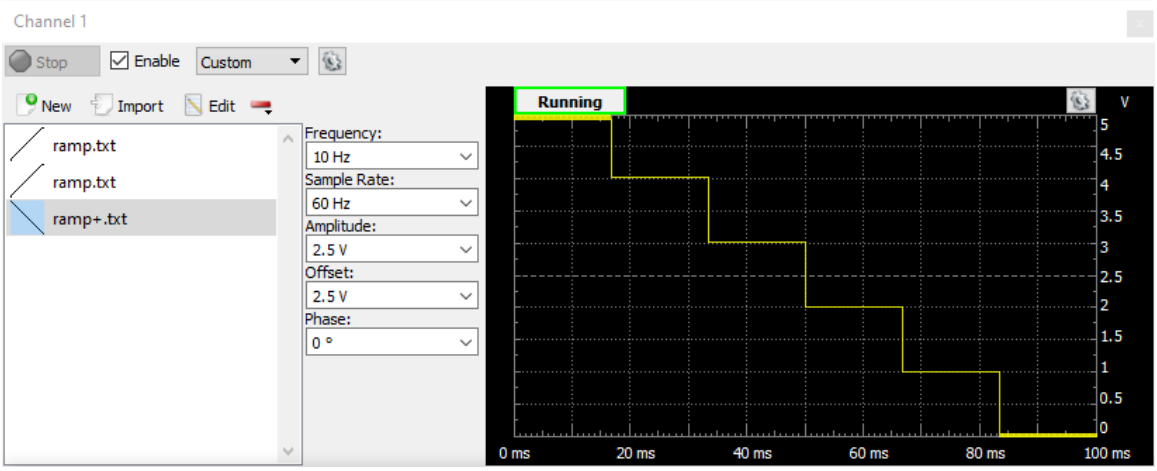


Fig. 8. The settings of the waveform generator #1.

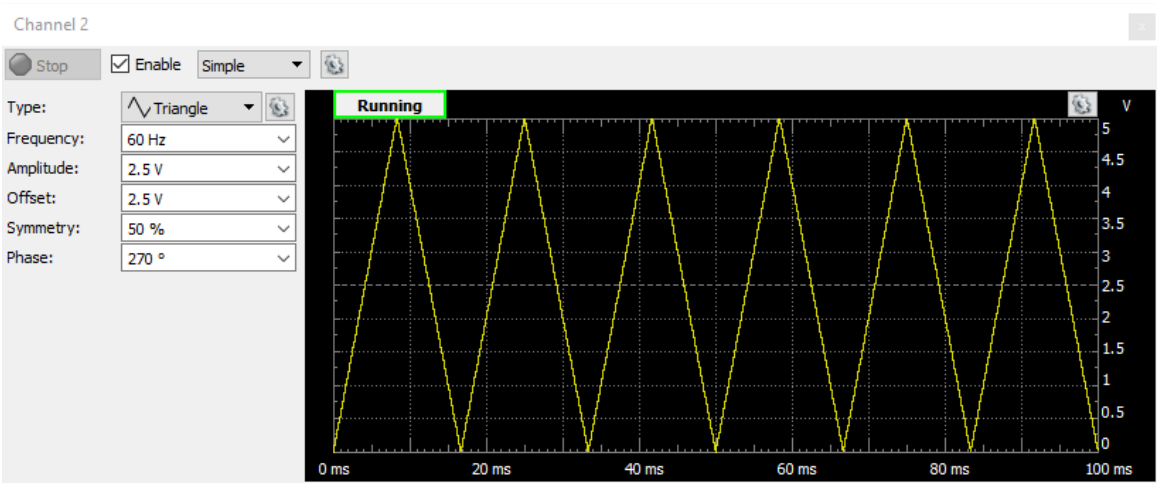


Fig. 9. The settings of the waveform generator #2.

Run the oscilloscope using exactly the same settings, e.g., time base, offset, range, as shown in the following figure. Click “View”, “Add XY”.

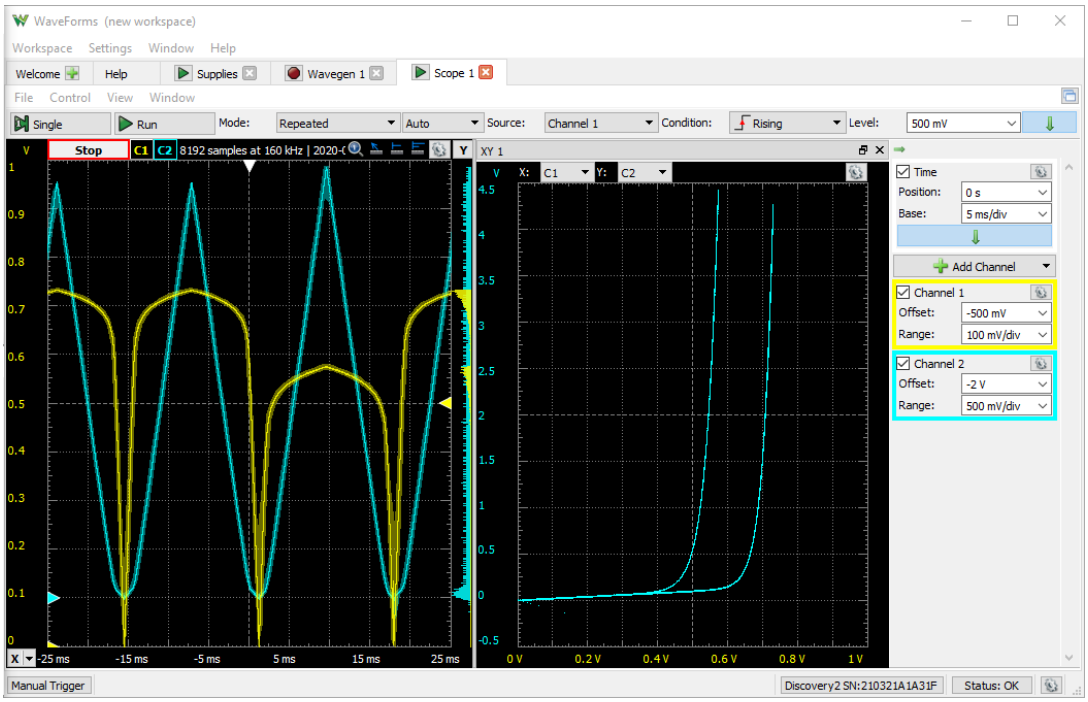


Fig. 10. The I_C versus V_{BE} characteristics of a transistor.

The plot on the right-hand side is the transistor input characteristics. The horizontal axis is V_{BE}. The vertical scale corresponds to I_B. Each unit is 10 μA because a 100-kΩ resistor is used in the circuit. Click "File", "Export" to save the plot and data. There are two curves in the plot. From left to right, they correspond to a V_{CE} of 0 V and >1 V, respectively. In other words, all curves with V_{CE}>1 V merge into one curve.

Similar to how the transistor is characterized, one can set up the instrument module to obtain characteristics of the n-MOSFET in CD4007 as shown below.

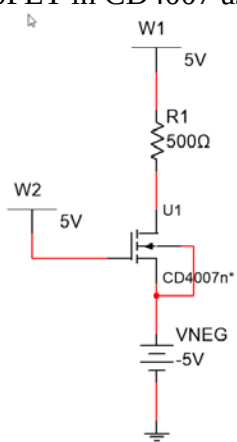


Fig. 11. The FET characterization circuit.

For the output characteristics, waveform generator W_1 produces a triangular wave sweeping between -5 V and 5 V. Waveform generator W_2 produces a step signal with the following voltages: -5 V, -3 V, -2 V, -1 V, 0 V, and +1 V. Oscilloscope channel #1 monitors V_{DS} and channel #2 monitors I_D., i.e., the voltage across the 500 Ω resistor, R_1. The following plot is obtained.

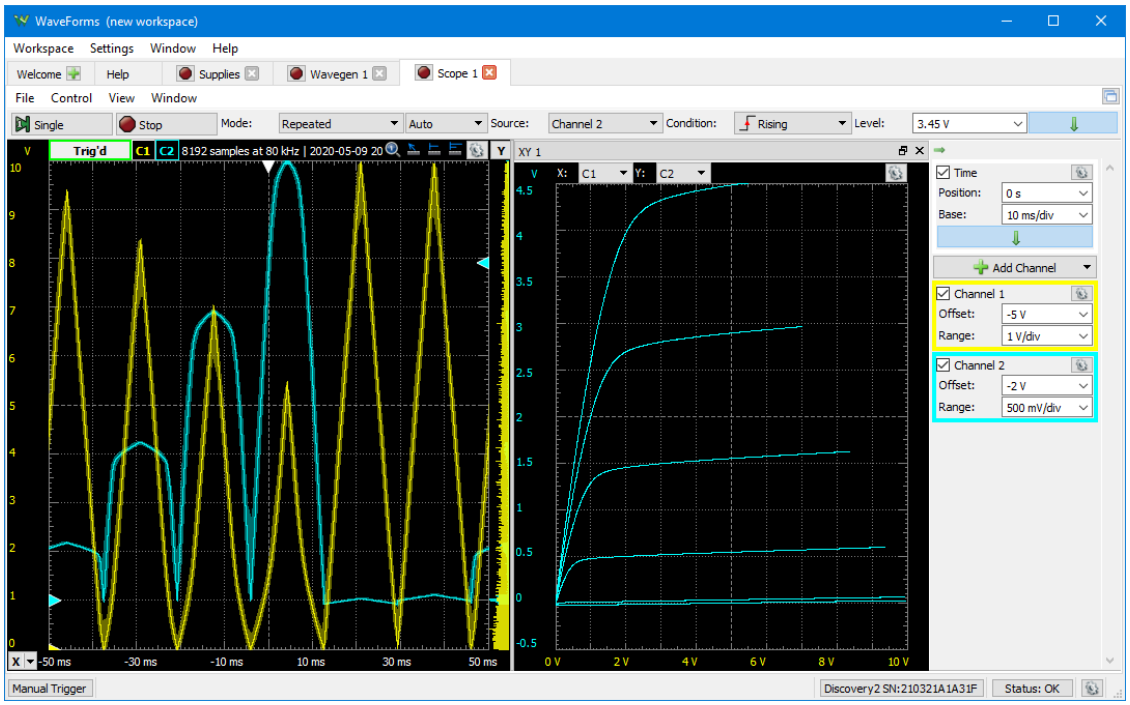


Fig. 12. The I_D versus V_{DS} characteristics of an FET.

There are six curves for the drain current, I_D versus V_{DS}. From bottom to top, they correspond to the following V_{GS} values: 0 V, 2 V, 3 V, 4 V, 5 V, and 6 V. Please note that vertical scale is in 2 mA unit because R_1 is 500 Ω; not 1 kΩ.

To obtain the input characteristics, waveform generator W1 is set for generating a dc offset voltage of +5 V. Waveform generator W_2 produces a triangular wave sweeping between -5 V and 5 V. Oscilloscope channel #1 monitors V_{GS}. Oscilloscope channel #2 monitors the drain current, I_D. Shown below is the input characteristics.

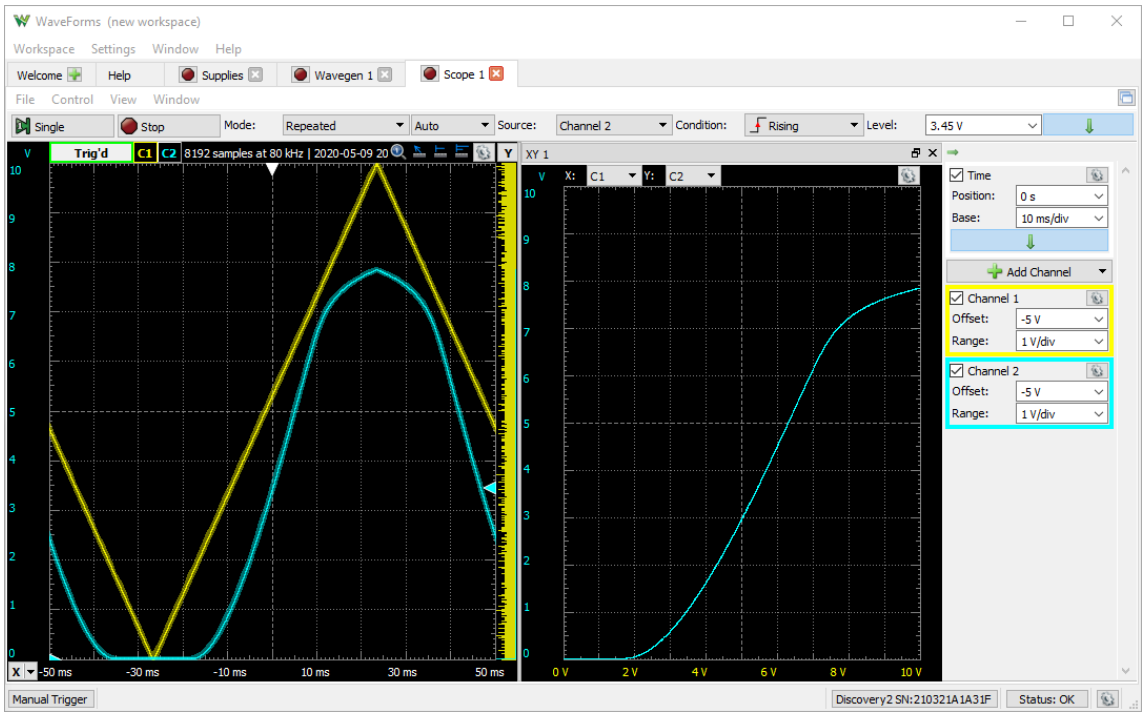


Fig. 13. The I_D versus V_{GS} characteristics of an FET.

The current starts to rise shortly before 2 V and starts to saturate when the V_{GS} is above 7 V due to reduced V_{DS} and *W1* at high current.

IV. Fast Fourier Transform (FFT)

In principle, with a sinusoidal input, a linear amplifier should produce also a sinusoidal output. In reality, all amplifiers are affected by device nonlinearity and produce distorted waveforms when the input, hence, output, becomes large. Distortion in the time-domain waveform leads to harmonics in the spectrum. With a 1-kHz, sine wave at input, the amplifier not only produces a large output at 1 kHz, it also generates harmonic components at 2 kHz, 3 kHz, 4 kHz, etc.

Characterizations in the spectral domain can be performed by using a spectrum analyzer which is a dedicated instrument. With a digitized waveform, spectral analysis can also be performed by using fast Fourier transform (FFT). There are plenty references and examples available online about FFT using Excel. The key is to know how to translate the time step and the number of data points to frequency markers. Digital oscilloscopes and digitizers, such as, ADALM2000 or Analog Discovery 2, have FFT capability built in.

To observe waveform distortion, one needs to increase the amplitude of the sinusoidal input until waveform distortion occurs at the output as shown below. The input signal is

shown in cyan color with 100 mV scale and the output signal is shown in yellow with 2 V scale. The peak-to-peak output voltage is very close to the 5-V power supply voltage.

Fig. 1. The input waveform in cyan and output waveform in yellow of a BJT amplifier.

If the waveform distortion occurs only at either the top or the bottom, you need to adjust the bias condition of the amplifier. Once the bias condition is optimized, the distortion should be present at both extremes as shown above.

To improve the resolution of FFT, one needs to adjust the time base so that many cycles are displayed. For the 1-kHz input, increase the time base to 20 msec/div. The next step is to invoke FFT. In Analog Discovery 2, this is done by clicking View, FFT. In a digital oscilloscope, you need to invoke the math function and select FFT. Both horizontal and vertical scales of the spectrum can be adjusted in Analog Discovery 2. For digital oscilloscope, you can adjust the time base and the vertical sensitivity. Please read the oscilloscope manual for details. Shown below is the spectrum displayed by Analog Discovery 2.

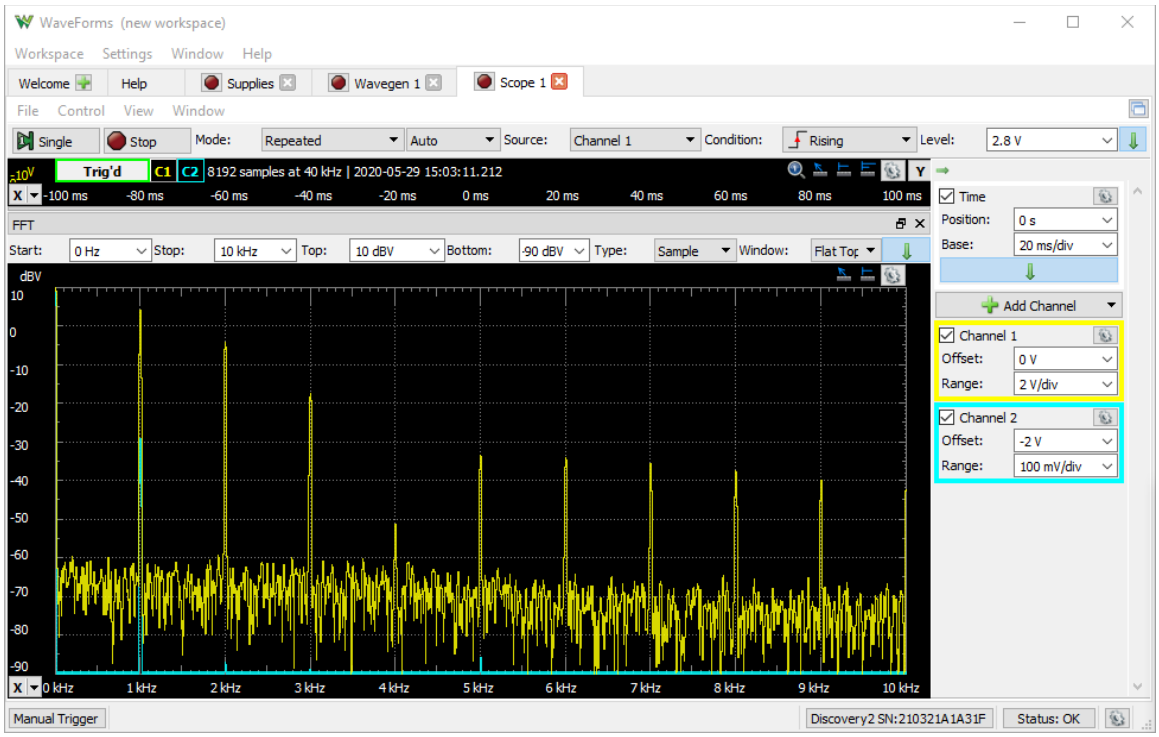


Fig. 2. The spectra of waveforms.

The fundamental frequency is at 1 kHz. Harmonics up to 10 kHz are shown. The horizontal scale is self-explanatory. The vertical scale requires some explanation. The vertical unit dBV means decibel in reference to 1 V. In the log scale, $dB=10\cdot\log_{10}(Signal/Reference)$. A signal with an amplitude of 1 V is represented by 0 dBV. A signal of 10 V is represented by 10 dBV; 100 V, 20 dBV; etc. By setting the top at 10 dBV and the bottom at -90 dBV, each division is 10 dB. The second harmonic at 2 kHz is approximately -8 dB below the peak at the fundamental frequency, 1 kHz. In other words, the second harmonic is approximately 16% of the fundamental peak. If you gradually reduce the amplitude of the input signal, you will observe that the harmonic distortion becomes less and less. In electronic systems, it is usually the last stage, power amplifier which contributes dominantly to the harmonic distortion.

You can also use the build-in spectrum analyzer to see the spectrum. Click “Welcome” and “Spectrum” to see the spectrum.

V. Network Function

Frequently, we need to characterize the frequency response of circuits, such as, the throughput of a filter and the gain of an amplifier. From the measured data, one can generate the Bode plot.

Analog Discovery 2 along with Waveforms can generate the Bode plot automatically using the network function. However, you can't rely on the default setting. You need to know how to set up the parameters correctly. Otherwise, the plot generated by Waveforms could be grossly misleading.

Let's consider an operational amplifier with a gain of -10 as an example. First, you need to verify that the circuit is working properly by using the oscilloscope. The OP27 chip in the Analog Parts Kit is used along with 1 kΩ and 10 kΩ resistors. Power supply is set at +5 V and -5 V. In order not to reach the saturation voltage, the waveform generator is set at 0.1 V amplitude and 1 kHz frequency. Here are the waveforms.

Fig. 1. The input waveform in yellow and output waveform in cyan color of an operational amplifier.

Waveforms confirm that the circuit is working properly with an input amplitude of 0.1 V. If the waveform generator amplitude were set to 1 V, the output waveform would have been clipped.

Only after knowing the proper amplitude setting without causing clipping, you can use the network function. Here is the network screen:

Fig. 2. The Bode plot of the operational amplifier at a gain of -10X.

You need to set the start frequency, e.g., 100 Hz, stop frequency, e.g., 1 MHz, samples, e.g., 100 or 200. More importantly, you need to set WaveGen amplitude to 0.1 V; not 1 V. You can click magnitude units to show the gain in linear scale. The alternative unit is dB scale. Since it is a -10X amplifier, a range of 10X is fine. The cyan trace is the output and the yellow trace is the input. If you want to use cursor, click X at the lower left corner to get the cursor. You can point the mouse to the first cursor and drag it to 1 kHz. You can point the mouse to the second cursor and drag it to a frequency at which the gain is near 7. Two frequencies show up at bottom, the first cursor frequency and the difference frequency between two cursors. The OP27 operational amplifier with a gain of -10X has a -3dB frequency around 435 kHz. The lower half of the screen shows the phase. Spikes at low frequency in the phase plot are spurious, i.e., not valid or without any physical origin. You should not pay any attention to them.

After changing 10 kΩ resistor to 100 kΩ, the -100X amplifier is in operation. First, check the waveforms to confirm that the amplifier is working properly. In order to avoid waveform clipping, set the input amplitude to 0.01 V. You can also use a voltage divider. With input amplitude at 0.01 V, here are the waveforms.

Fig. 3. The input waveform in yellow and output waveform in cyan color of an operational amplifier at a gain of -100X.

Noise is present as indicated by the fuzzy yellow trace. Amplifier has an offset, i.e., more positive than the negative. Nevertheless, the output waveform is not clipped, hence the offset should not be an issue in characterizing the frequency response. you can always null the offset by adding a potentiometer. Here is the network screen:

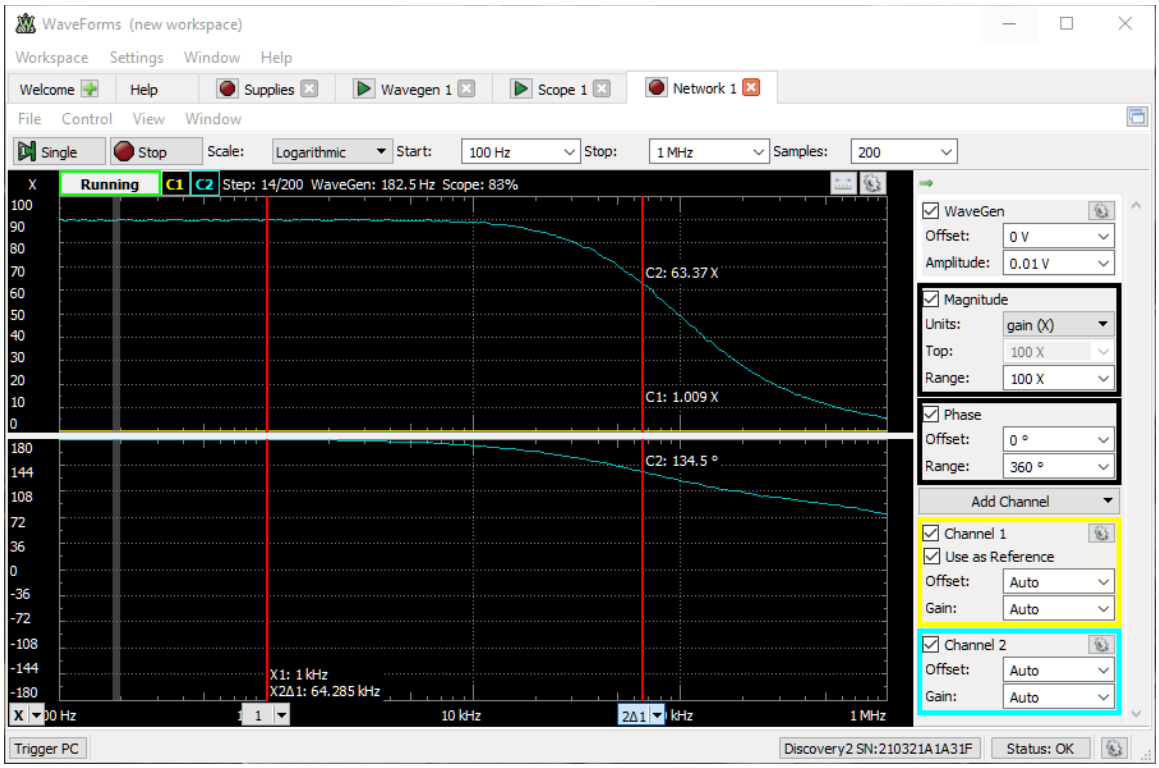


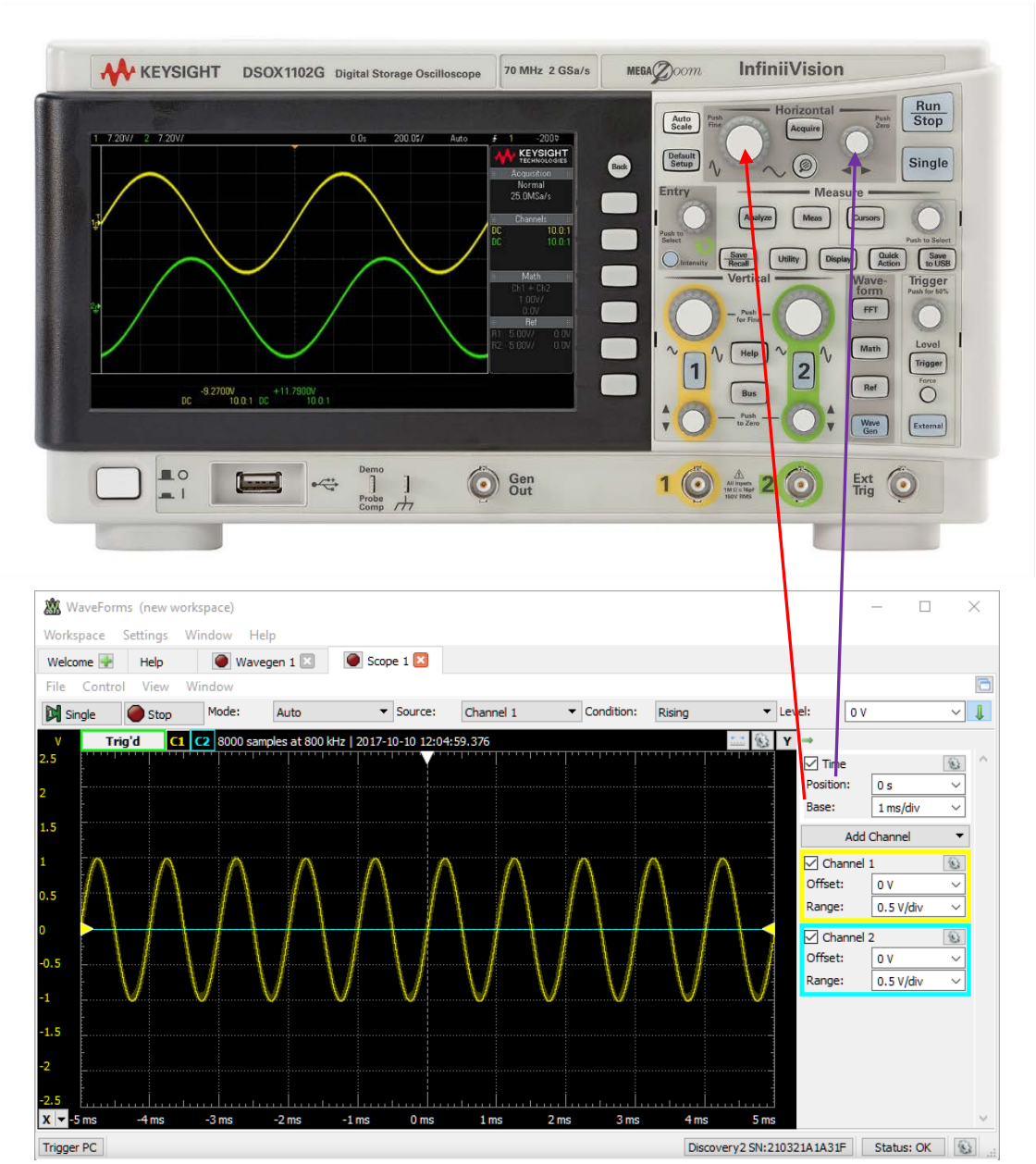
Fig. 4. The Bode plot of the operational amplifier at a gain of -100X.

Please note that WaveGen amplitude is set to 0.01 V and range to 100X. The -3dB point is down to 65 kHz.

Please note that automated measurements can save you time. However, you can only trust automated measurements if you know how to set parameters correctly. Furthermore, automated oscilloscope peak-to-peak voltage measurements may not be of high accuracy when noise is present. That is the reason why you see a gain of 90 instead of 100 in the -X100 amplifier.

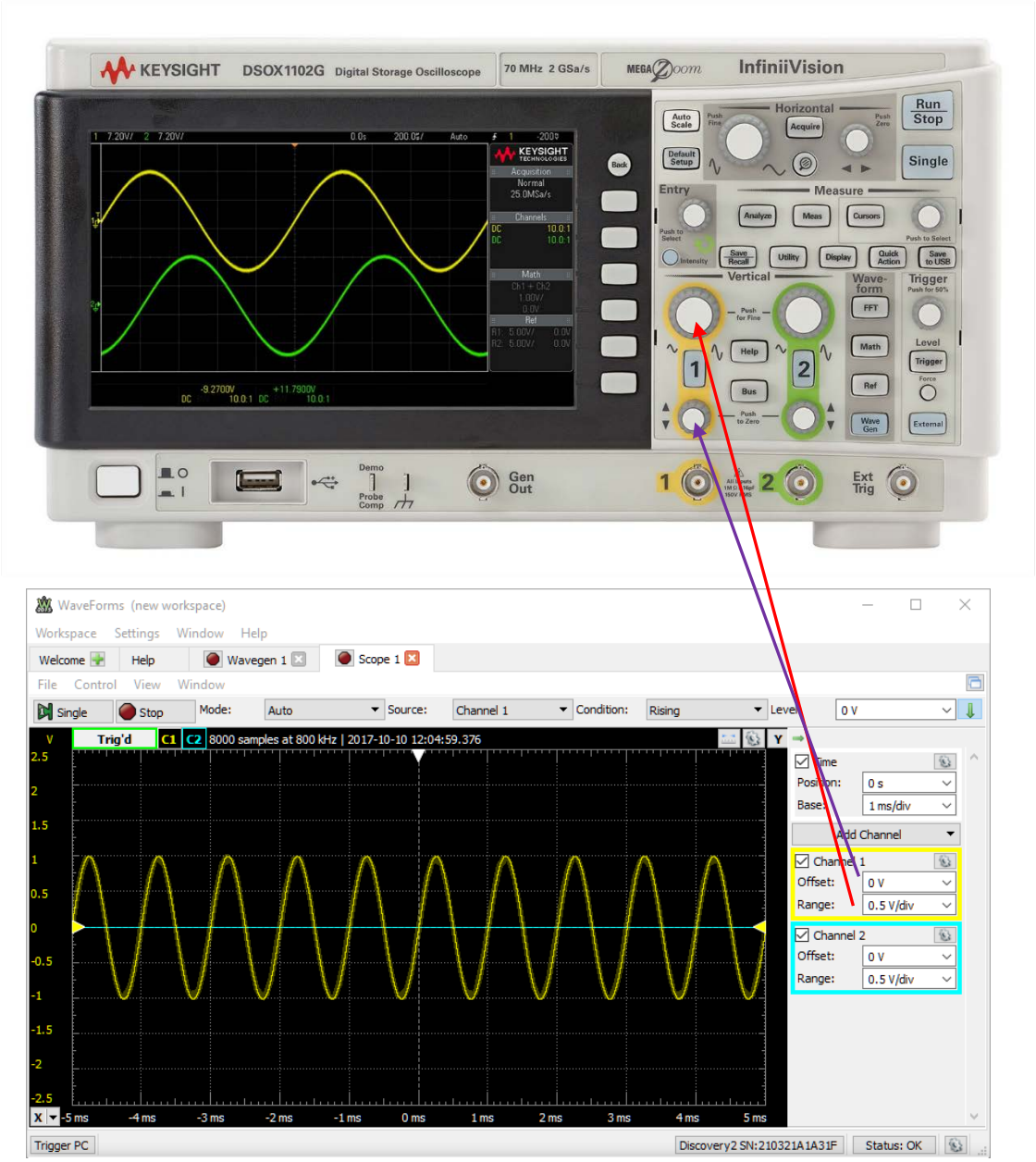
VI. Migration from Multi-Function Module to Benchtop Instruments

When instruments are available, they are preferred to personal modules because of better performance. We will show the most crucial one-to-one correspondences between Analog Discovery 2 and DSOX1102G oscilloscope, 33120 A function generator and the Instek laboratory power supply to facilitate the transition.



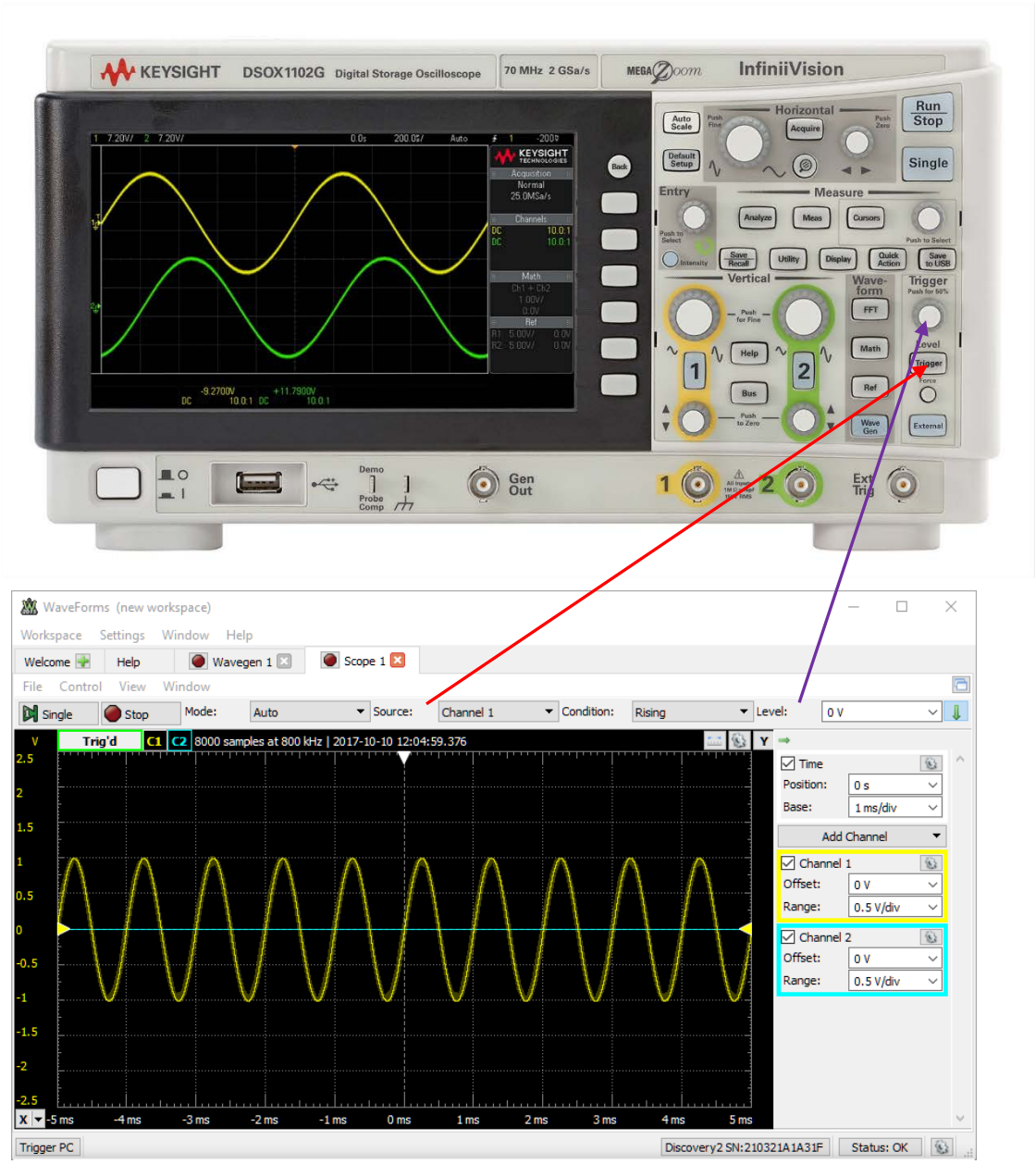
Time base adjustment is used to change the time scale, i.e., msec/div.

Position adjustment is used to move the waveform right or left.



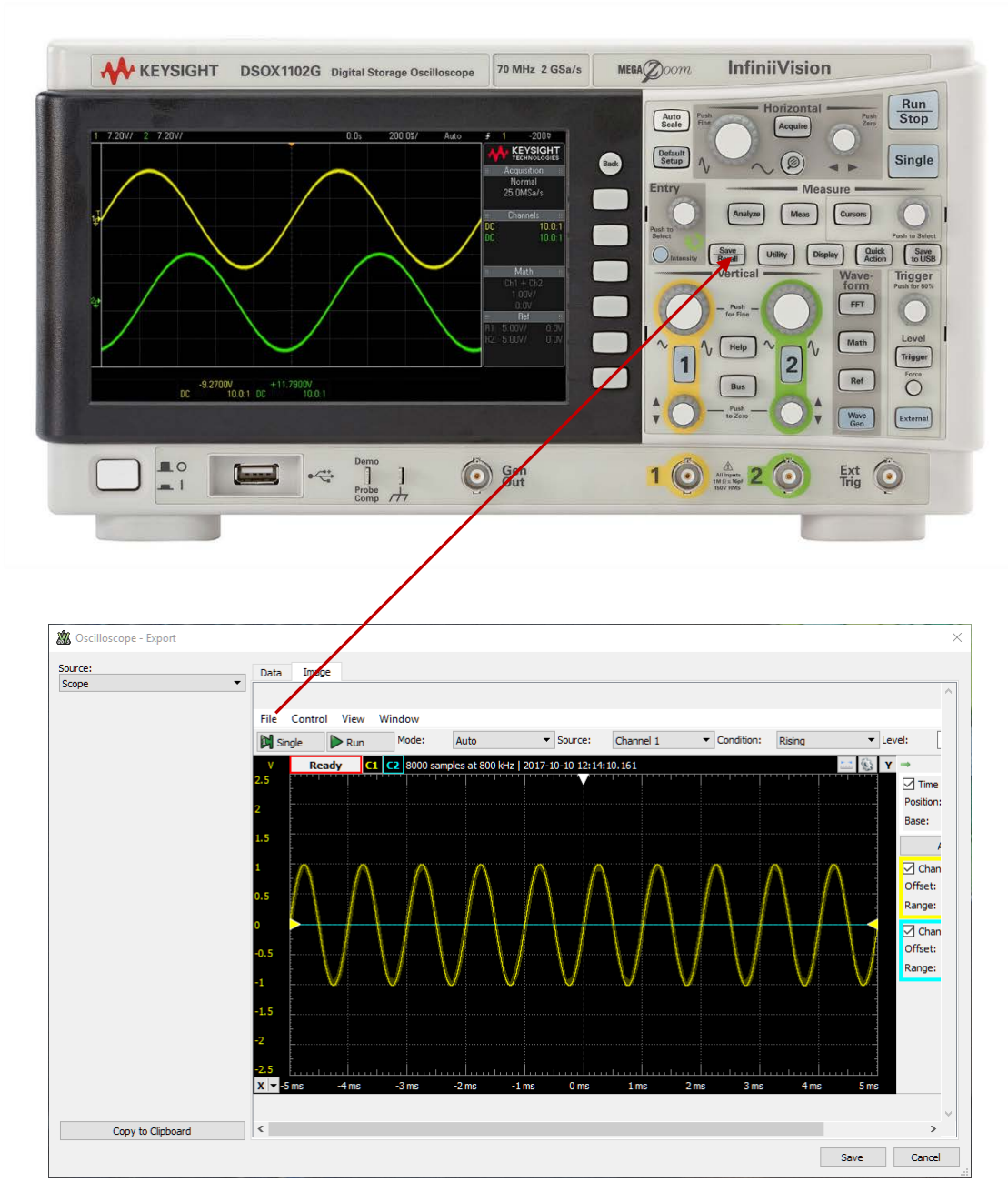
Range adjustment is used to change the vertical sensitivity scale, i.e., V/div.

Offset adjustment is used to move the waveform up or down.

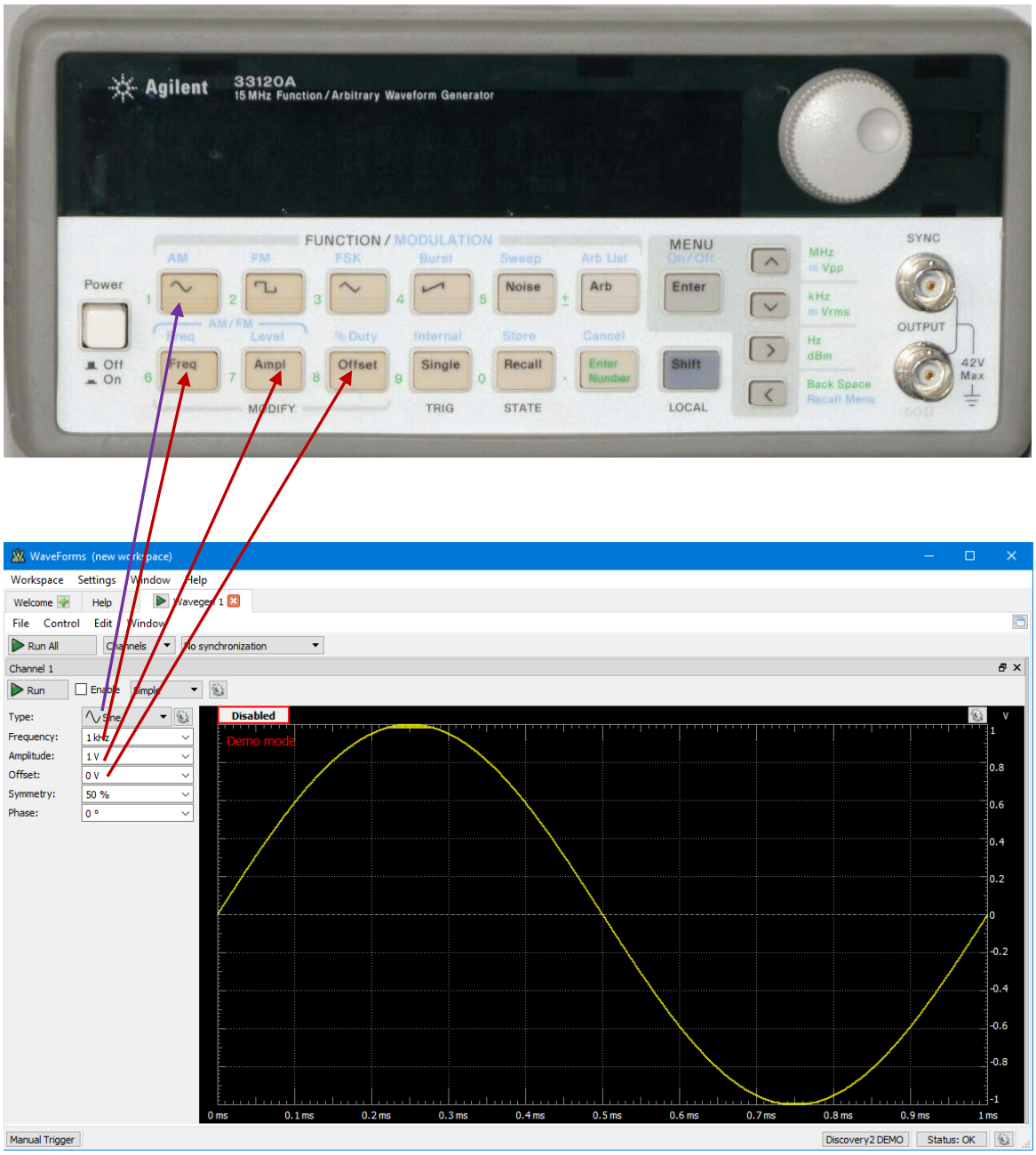


The trigger button is used to select the trigger source and its settings, e.g., rising or trailing edge.

The trigger level knob is used to set the voltage level of the trigger.

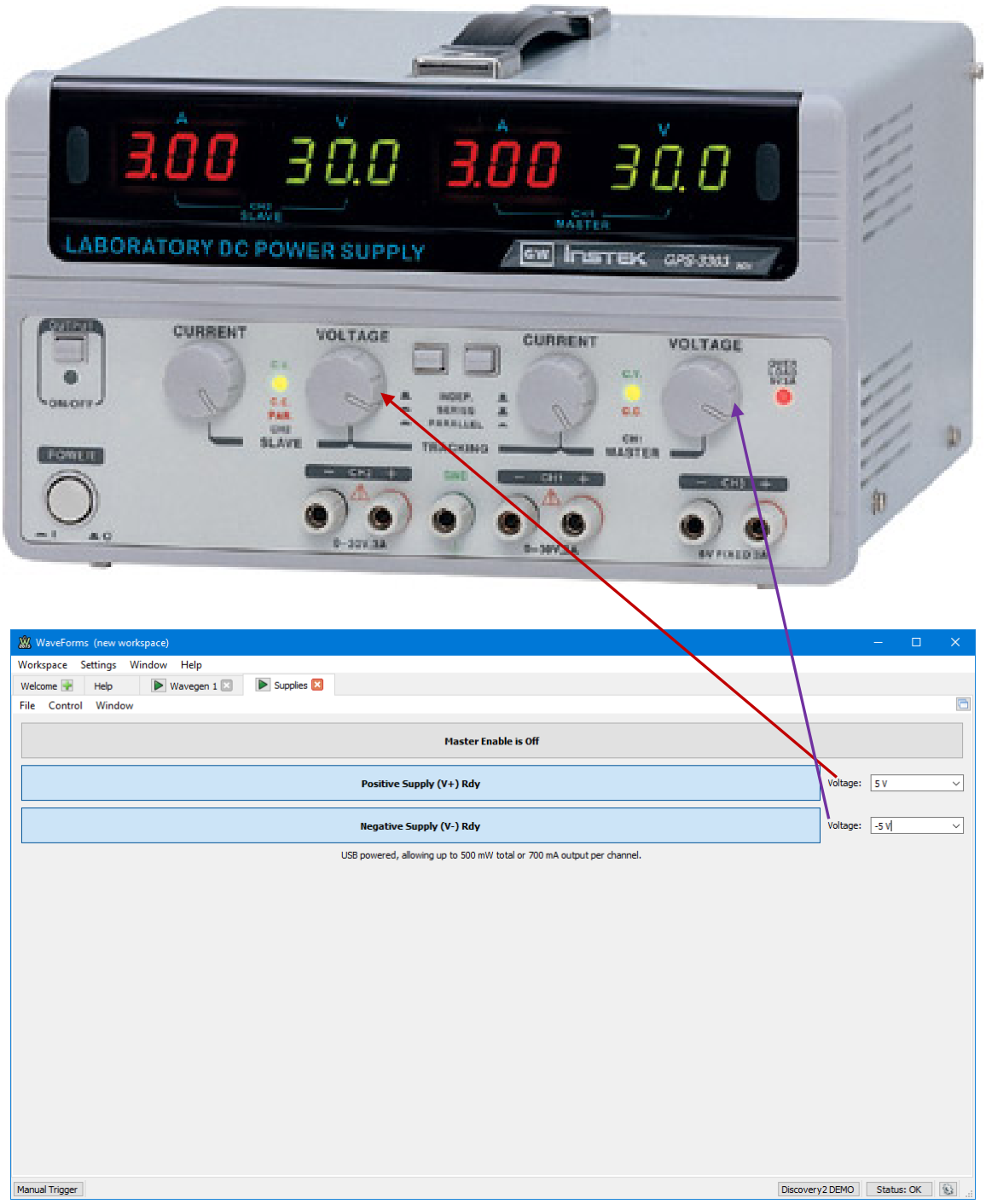


One can save waveforms and data by pushing the “Save/Recall” button on the oscilloscope. Likewise, there is the file, export feature in Analog Discovery 2.



You can adjust the frequency, amplitude, and offset.

You can choose the waveform shape.



You can set the voltage of the positive power supply.

You can set the voltage of the negative power supply.