ELSEVIER

Materials Science and Engineering B37 (1996) 17–24

MATERIALS SCIENCE & ENGINEERING B

Monte Carlo simulation of the growth of semiconductor quantum wires

Vladimir Mitin*, Saulius Keršulis

Department of Electrical and Computer Engineering, Wayne State University, Detroit, MI 48202, USA

Abstract

The results of Monte Carlo simulation of the growth of semiconductors on (001), (111), and (411) surfaces are presented. The simulation model includes tetrahedral lattice coordination of material, atom–atom interactions out to second-nearest neighbors, and surface reconstruction effects. The simulation results show that the transition from rough to smooth growth mode for the (111) surface occurs at lower temperatures than for growth on the (001) surface, indicating a higher diffusion coefficient of adatoms on the (111) surface in comparison with (001). The results of simulation growth on the (411) surface do not show any essential difference from (001) growth. The formation of structures on the top of ridges formed on (001) and (411) planes has been simulated. The (111) side walls were found to be flat in both cases owing to a substrate temperature which is high enough to ensure high mobility of adatoms on the (111) surface. The (001) and (411) surfaces on the top of the ridges showed approximately the same quality and the only difference found was in their shape, which was symmetric for the (001), and not symmetric for the (411) case.

Keywords: Monte Carlo simulation; Semiconductors

1. Introduction

In recent years, there has been increasing interest in the molecular beam epitaxy (MBE) growth of low-dimensional III–V semiconductor structures on patterned substrates. This interest has been motivated by the creation of low threshold current laser structures and other optical devices [1–4]. Understanding of the atomic processes during growth is crucial for the fabrication and control of high quality semiconductor structures. Many investigations in this area have been carried out to elucidate the growth mechanism.

Patterning of (100) oriented GaAs substrates with grooves and ridges has been studied experimentally [5–13].

MBE growth of GaAs, AlAs, and AlGaAs on V-grooved GaAs substrates was investigated in Refs. [5,6]. V-grooves were aligned along the [110] direction on (001) GaAs substrates and had V-shaped profiles with (111)A sidewalls as a result of anisotropic etching. When GaAs layers were grown on the V-grooved substrates, an exponential change in thickness of GaAs layers on the (001) surface near the edge of the (111)A sidewall was observed, while the AlAs and AlGaAs layers showed no such exponential growth [6]. This effect was explained in the following way. When GaAs is grown on the V-grooves, the probability of incorporation of a Ga atom on the (111)A surface is relatively low and its diffusivity is relatively high, so that Ga atoms migrate easily from sidewalls to the (100) surface. In the case of AlAs and AlGaAs, since the diffusivity of Al atoms is much smaller and atom incorporation, i.e., the growth rate, is greater on (111)A surfaces, intersurface migration is very small. The same effect of significant Ga atom migration on the Ga(111) surface was observed in [7–11]. In [9,10], the migration length of a Ga atom on a GaAs(111) sidewall was found to be of the order of several micrometers. Using this effect of the different growth behavior of GaAs, AlAs, and AlGaAs, multiple crescent-shaped GaAs quantum wires about (140–160 Å) × (400–500 Å) in size have been grown successfully at the bottom of the V-grooves [5,6].

Facetted growth of GaAs/AlGaAs epilayers on ridges has been studied [12,13]. Rectangular ridges aligned along the [011] direction on a (001) surface were

* Corresponding author.

SSDI 0921-5107(95)01451-9

formed through a photoresist mask by reactive ion etching, and (GaAl)As layers were regrown on the ridges by MBE. (111)B planes on both sides of the ridge as well as the (100) facets in the center of the ridge were formed. As a result of the enhanced migration of Ga atoms from (111)B planes to (100) facets, the GaAs layers growing on the (100) planes on top of the ridge were thicker and they were embedded completely in AlGaAs. With decreasing ridge width, the (111)B planes restrict the formation of (100) facets on top of the ridges, resulting in triangular shaped structures. In this way, quantum wires were grown [12].

There are a very small number of publications devoted to Monte Carlo (MC) simulation of the growth of such semiconductor structures. In [14,15], the growth kinetics on a (100) surface with a facetted V-groove was studied by MC technique. The model of facet growth during MBE included growth of a simple cubic lattice structure in which vacancies and overhangs are forbidden, the so-called solid-on-solid (SOS) approximation [16]. Second-nearest-neighbor interaction was taken into account to incorporate facetting behavior. The effective growth rates on (100), (111)A, and (111)B surfaces were calculated and good qualitative agreement with experimental data of Ref. [9] was obtained.

The growth of GaAs quantum-well wires on vicinal surfaces was studied by MC simulation in [17,18]. An optimum regime within which the quality of quantum-well wire is maximum was obtained. The dependence of the quality of quantum-well wires on the direction of misorientation from the (100) plane was considered.

2. The model

Our simulation model is an SOS model which deals with the tetrahedral lattice structure of semiconductor material where both the nearest neighbors and the second-nearest neighbors are taken into account. Incorporation of this structure in our simulations of growth on the (100) plane is very similar to that proposed in [19]. A set of two two-dimensional arrays $L(x, y)$ and $R(x, y)$ is used. The $L(x, y)$ array indicates the lateral position on the surface and the height of surface atoms relative to an arbitrary substrate reference plane. The $R(x, y)$ array is used to describe the effect of surface reconstruction. We also use this technique in our simulations growth on the (111) plane.

Four kinetic processes (deposition of the atom onto the surface, the migration of this atom on the surface, the evaporation of deposited atoms from the surface, and surface relaxation) are taken into account. The complexity of these kinetic processes is simulated using the Arrhenius rate equation for each of these processes: $R = R_0 \exp[-n_1 E_1 + n_2 E_2)/kT]$, where n_1 and n_2 are the numbers of first- and second-nearest neighbors, and E_1 and E_2 are the first- and second-nearest-neighbor interaction energies respectively.

The (2×1) surface reconstruction process on the (100) plane of the semiconductor is simulated in a way similar to that used in Ref. [8], i.e. the following is assumed; (1) dimer formation occurs spontaneously between two undimerized surface atoms located in the same layer at adjacent columns, and which have no upper nearest-neighbor atoms; (2) impinging atoms always break underlying atoms to chemisorb on the surface; (3) "flip" events, in which a dimerized atom "swaps" partners by first breaking the dimer bond to an already-existing partner and then reforms a new dimer with the undimerized atom in the opposite direction, take place during growth. The kinetic flipping rate is calculated according to the same Arrhenius-type equation, in which the activation energy E_f depends on the configuration of neighboring dimers and can be expressed as $E_f = E_d - mE_{fi}$, where $E_f = 2$ eV is the dimer energy in the ideal (2×1) reconstruction, $E_{fi} = 0.2$ eV is an energy term used to describe the influence of the configuration of neighboring dimers on the flip rate on lattice site i, and m is an integer having a value in the range 0–4, depending on the presence and orientation of adjacent dimers. The case when $m = 0$ represents the most stable perfect (2×1) reconstruction with the lowest rate of flip events. In cases $m = 1 \ldots 4$ we have less stable dimer pairs with higher probabilities of flip events.

The MC algorithm used is similar to the fast MBE growth algorithm of Maksym [20]. According to this algorithm, the time, type, and site of each of the four events mentioned above are chosen randomly with a probability of occurrence that depends on the kinetic rates for the individual events at each lattice site.

The time for the event to occur is obtained from the total kinetic rate:

$$R = \sum_{i=1}^{n} (R_{di} + R_{hi} + R_{ei} + R_{fi})$$

where N is the number of surface sites, R_{di}, R_{hi}, R_{ei}, and R_{fi} are kinetic rates of deposition, hopping, evaporation, and flip events respectively. The time t between successive events is determined from

$$t = -\frac{1}{R} \ln r$$

where r is a random number distributed uniformly between 0 and 1.

The conditional probabilities of the event being deposition, hopping, evaporation, or flipping are R_d/R, R_h/R, R_e/R, and R_f/R respectively, where R_d, R_h, R_e, and R_f are the total rates of deposition, hopping, evaporation, and flipping:

$$R_d = \sum_{i=1}^{N} R_{di} \quad R_h = \sum_{i=1}^{N} R_{hi} \quad R_e = \sum_{i=1}^{N} R_{ei} \quad R_f = \sum_{i=1}^{N} R_f$$

Numerically, the type of event is selected with a second random number r_2. The event is hopping of an atom on the surface for $Rr_2 < R_h$, evaporation for $R_h < Rr_2 < (R_h + R_e)$, flipping for $(R_h + R_e) < Rr_2 < (R_h + R_e + R_f)$, and deposition for $Rr_2 > (R_h + R_e + r_F)$.

The site of event is located in a similar way. Thus, if hopping takes place the site is found by looking for the largest i such that

$$Rr_2 > \sum_{j=1}^{i-1} R_{hj}$$

The sites of evaporation and flipping are found by testing the inequalities

$$Rr_2 - R_h > \sum_{j=1}^{i-1} R_{ej}$$

$$Rr_2 - R_h - R_h - R_e > \sum_{j=1}^{i-1} R_{fj}$$

respectively. The x and y coordinates of the lattice site for the deposition of an adatom are determined randomly.

3. Results and discussion

For simulation of the growth of semiconductor quantum wires on the top of ridges formed on a (100) plane with (111) side walls, it is necessary to study the growth on these planes simultaneously. Using the model described in Section 2, we performed a set of computational experiments on the simulation of the growth of semiconductor material with tetrahedral lattice coordination on (001) and (111) planes.

First- and second-nearest-neighbor interaction energies are among the most important parameters in the simulations. Our choice of values was based on experimental data on the growth of Si(001) indicating the growth of high quality Si(001) surface at substrate temperatures above 650 °C [21–24]. The numerical values used in the simulation of the hopping kinetic process were chosen to be $E_1 = 0.6$ eV, $E_2 = 0.1$ eV. Energy terms for the evaporation event were taken to be $E_1 = 1.1$ eV, $E_2 = 0.2$ eV. The pre-exponential hopping rate or hopping attempt frequency R_0 was assumed to be $R_0 = 10^{13}\ s^{-1}$.

Most of the results presented here are for a 80×80 lattice with, typically, ten layers grown on the substrate. Most of our results are means of ten simulations run using different random number sets. For a given deposition rate (impinging flux density) of 1 monolayer s^{-1} (i.e. deposition rate of 6400 atoms s^{-1} for an 80×80 lattice) we changed the substrate temperature from 400 K to 900 K and compared the results of growth on different crystallographic planes.

For quantitative characterization of the quality of the growing material, we introduced the interface width (roughness) Δ [25]:

$$\Delta = \langle (h_i - \langle h \rangle)^2 \rangle^{1/2}$$

Here h_i is the height of the ith column of the structure. The angular brackets denote an average over all surface sites. Δ is expressed in units of monolayers (ML).

In Fig. 1 we present the simulation results of (001) growth at different substrate temperatures for the deposition rate $R_d = 1.0$ ML s^{-1}. The temporal evolutions of interface width (roughness) Δ at substrate temperatures $T = 700$, 750, 800, and 900 K are shown. It can be seen that at $T = 700$ K the growth is clearly rough three-dimensional with Δ increasing over time and many (five or six) monolayers growing together at the same instant (Fig. 2(a)). The temperature range $T = 750 \ldots 800$ K can be called intermediate between the rough and smooth growth modes. In this temperature regime the interface width tends to saturate with time (especially at $T = 800$ K), and has a much lower value than for $T = 700$ K. At $T = 900$ K, we observe smooth two-dimensional growth with Δ saturated with time, which is in good agreement with experimental data on the growth of Si(001) [24,25]. Moreover, the temporal oscillations of Δ can be seen at the beginning of growth at $T = 900$ K, indicating a layer-by-layer growth mode. The temporal evolution of filling of monolayers also indicates layer-by-layer growth at $T = 900$ K (Fig. 2(b)).

The results of simulation of growth on the (111) surface at the same deposition rate ($R_d = 1.0$ML s^{-1}) and using the same activation energies as for the (001) surface are depicted in Figs. 3 and 4. Fig. 3 represents the temporal evolutions of interface width (roughness) Δ of the (111) surface at substrate temperatures $T =$ 400, 450, 475, and 500 K. We can see from this

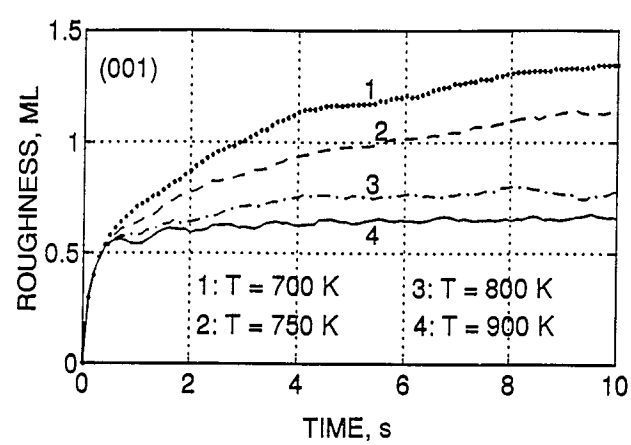

Fig. 1. Temporal evolution of the surface roughness during deposition of ten monolayers of Si onto a (001) surface at different substrate temperatures (deposition rate $R_d = 1$ ML s^{-1}); curves 1, 2, 3, and 4 correspond to substrate temperatures 700, 750, 800, and 900 K respectively.

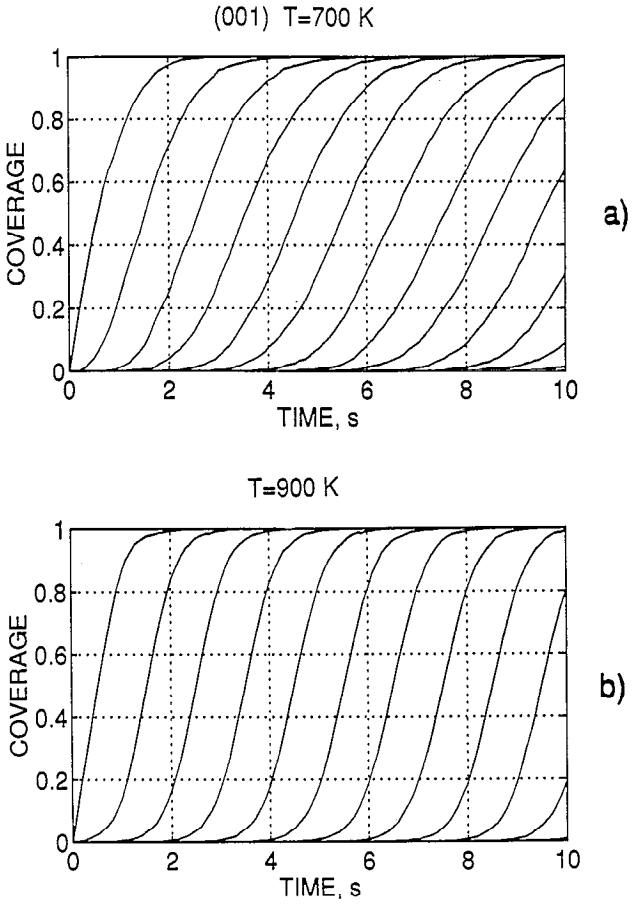

Fig. 2. Filling of layers during deposition of ten monolayers of silicon onto a (001) plane at $T = 700$ K (a), and $T = 900$ K (b).

figure that the temperature range $T = 450 \ldots 475$ K is intermediate between the rough and smooth growth modes. Temporal oscillations of Δ at temperatures $T = 475$ K and 500 K can be clearly seen in this graph. The interesting peculiarity of these oscillations is that the period of the oscillations is about 2 s, which corresponds to the time of deposition of one complete

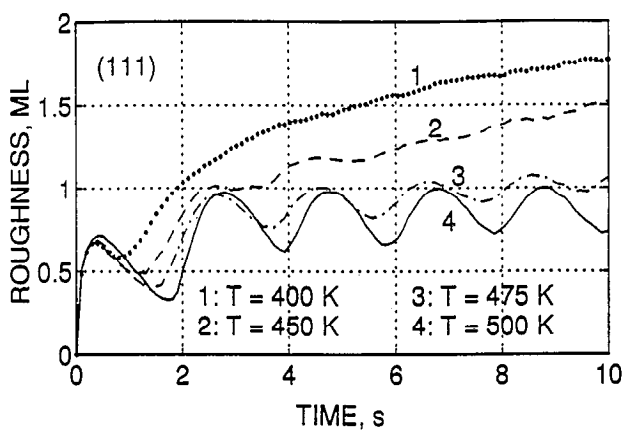

Fig. 3. Temporal evolution of the surface roughnesss during deposition of ten monolayers of Si onto a (111) surface at different substrate temperatures (deposition rate $R_d = 1$ ML s^{-1}); curves 1, 2, 3, and 4 correspond to substrate temperatures 400, 450 475, and 500 K respectively.

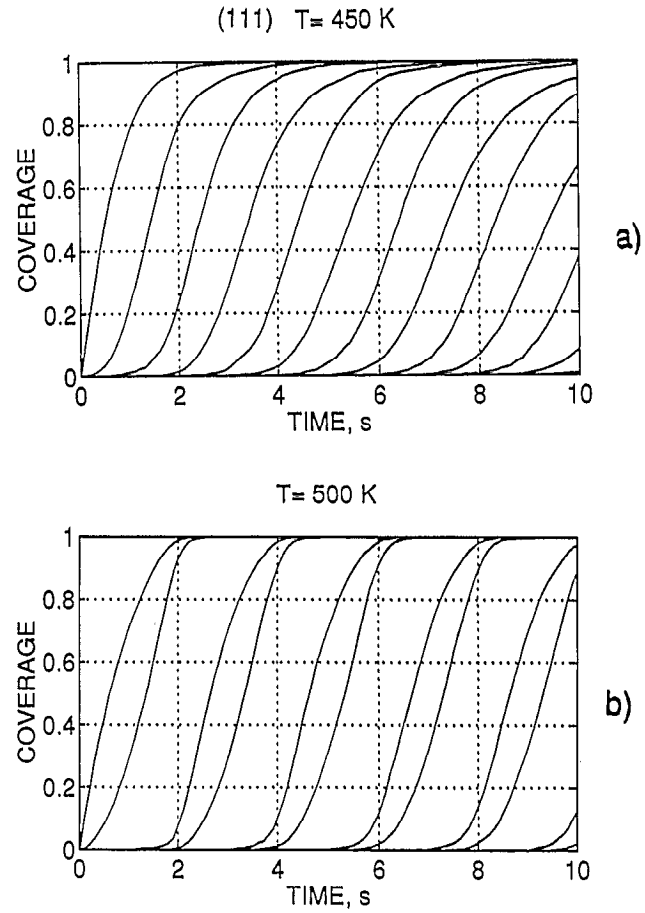

Fig. 4. Filling of layers during deposition of ten monolayers of silicon onto a (111) plane at $T = 450$ K (a), and $T = 500$ K (b).

bilayer at a deposition rate of 1 ML s^{-1}. So, in this temperature range we observe not monolayer-by-monolayer growth (as was found for the (001) surface) but a bilayer-by-bilayer growth mode, which corresponds to experimental observations [26–28]. The results of filling of layers at two different temperatures (450 K and 500 K) also show a bilayer growth mode (Fig. 4). Fig. 4(b) shows the growth of high quality (111) material. In this case, not more than two bilayers are being filled at the same time. As follows from this figure, filling of the next bilayer starts just after the previous bilayer has been almost filled out.

The main difference between (111) and (001) surfaces of a tetrahedral lattice structure is that in the [111] direction there are two types of layer while in the [001] direction all layers are equivalent. Atoms on one type of layer of the (111) surface have three nearest neighbors underneath, while atoms on the other type of layer have only one nearest neighbor underneath them. Therefore, the hopping rates on these two types of surface are different. For illustration, in Fig. 5 we show the hopping rates for an atom on three ideal flat surfaces: a (001) plane for an atom having two first-nearest and four second-nearest neighbors (dashed curve), a (111) surface with one first-nearest and three

second-nearest neighbors (upper solid curve), and a (111) surface with three first-nearest and three second-nearest neighbors (lower solid curve). A large difference in the hopping rates on the two types of (111) surface (of the order of 10^8–10^{13} s^{-1}) is clearly seen from this figure.

Comparison of the temporal evolution of the surface roughness Δ presented in Fig. 1 and Fig. 3 shows that the transition from rough to smooth growth mode for the (111) surface occurs at much lower temperatures than for growth on the (001) surface. At $T = 500$ K we observe intensive adatom motion on the (111) surface which causes the growth of high quality material. On the (001) plane the adatoms are almost immobile at $T = 500$ K (they have very low diffusion up to $T = 700$ K), and the growth here is rough and three-dimensional. This difference in growth on (111) and (001) surfaces corresponds to the experimental data of [7–11] where different migration lengths of Ga atoms on (100) and (111) surface were observed. This result implies that V-grooved structures or structures with ridges similar to those of [7–11] can be obtained in the growth of silicon-like semiconductor materials.

The results of simulation of growth of structures with ridges on top of the (001) plane with the (111) side walls at two different temperatures ($T = 700$ K and $T = 800$ K) are shown in Fig. 6. The dimensions of the lattice simulated were 40×20, and the deposition rate was 1 ML s^{-1}. Hopping rates on the (001) surface are lower than on one of the (111) surfaces (Fig. 5). That is why in the first stage of our simulations of the growth of quantum wires we assumed an infinitely large difference in these rates. Using this assumption we obtained flat (111) side walls at both temperatures. As we can see from Fig. 6(a) and Fig. 6(b), the only difference between the results is the quality of the top (001) surface

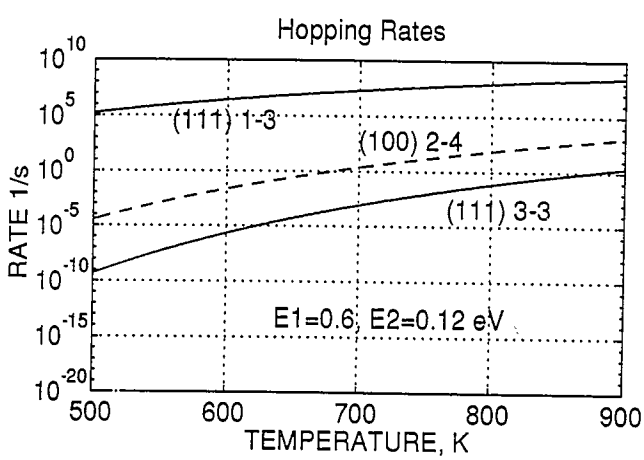

Fig. 5. Rates of hopping of an atom residing on a flat (001) surface with two first-nearest and four second-nearest neighbors (dashed curve), residing on a (111) surface with one first-nearest and three second-nearest neighbors (upper solid curve), and residing on a (111) plane with three first-nearest and three second-nearest neighbors (lower solid curve).

which is better at $T = 800$ K than at $T = 700$ K. The reason for this difference follows from Fig. 1 where the time dependence of the roughness of the (001) surface on substrate temperature is shown. It can be seen from Fig. 1 that the temperature $T = 700$ K corresponds to the conditions of rough three-dimensional growth of the (001) surface, while at $T = 800$ K the roughness is less and the quality of the growing surface is higher. The major result of our simulations is the formation of facets with (111) side walls with clear narrowing of the quantum wire during growth.

The formation of facets with (111) side walls and (001) surface on the top of the structure is also pronounced in the growth of quantum wires by deposition through shadowing mask. In these simulations we went beyond the assumption of an infinitely large difference in the hopping rates on different planes and simulated the actual hopping processes everywhere according to the Arrhenius expression. First we deposited five monolayers of Si onto an Si(001) surface with dimension 60×80 lattice sites. Then we started the deposition of Si atoms onto one region (30×80 lattice sites) of the already formed 60×80 site (001) surface at T = 800 K. Fig. 7 shows the front view of the surface configuration after the deposition of six additional monolayers onto the five monolayer thick Si(001) "buffer layer". The formation of (111) side walls of higher quality than the top (001) surface can be seen in the figure. After deposition of the buffer layer of Si(001) we can start the deposition of Ge atoms. In this way the growth of SiGe/Si can be investigated. Thus, or results demonstrate the possibility of growth of SiGe/Si quantum wires on ridge structures as well as by deposition through a shadowing mask. The experimental growth of such structures by local epitaxy through shadowing masks has been investigated intensively during recent years [29–31]. Our results of simulations of such structures will be published elsewhere.

The necessity of fabrication of semiconductor interfaces of higher quality than in (001) or (111) surfaces has led to attempts to grow semiconductor materials on (110), (311), (411) and other surfaces. In particular, the growth of GaAs/AlGaAs quantum wells on a GaAs (411)A facet was performed in [29]. The possibility of forming extremely flat and uniform GaAs–$Al_{0.3}Ga_{0.7}As$ interfaces using a (411)A GaAs substrate was reported in [32].

We have simulated the growth of a silicon-like semiconductor on the (411) surface. In Fig. 8 we present the simulation results of (411) growth at a substrate temperature T = 600 K for the deposition rate $R_d = 1.0$ ML s^{-1}. The temporal evolution of the interface width (roughness) Δ and filling of layers during the deposition of ten monolayers are shown in Fig. 8(a) and Fig. 8(b) respectively. It can be seen from this figure that at $T = 600$ K the growth is three-dimen-

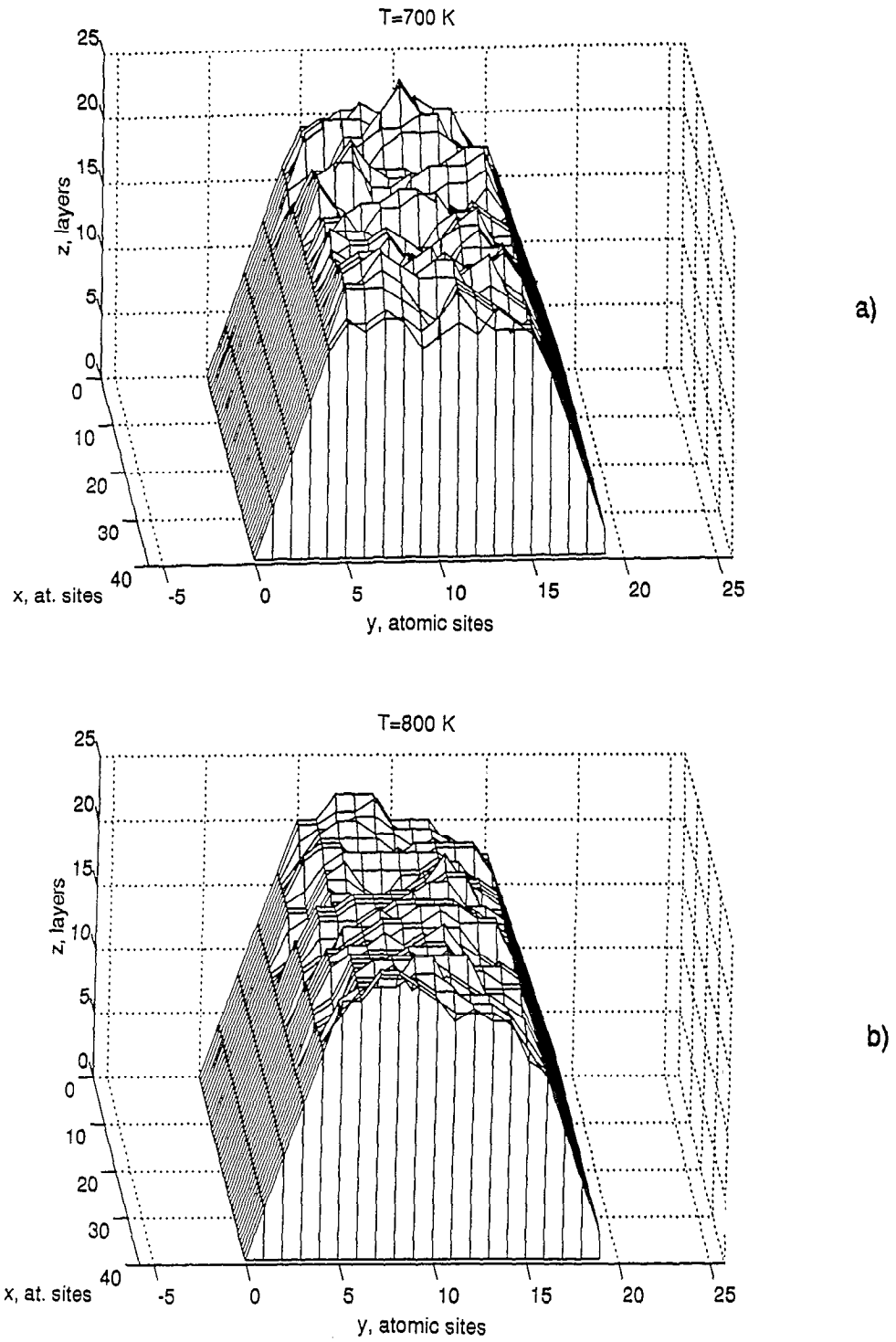

Fig. 6. Schematic representation of the structure with ridge formed on the top of a (001) surface with the (111) side walls grown at a substrate temperature $T = 700$ K (a) and $T = 800$ K (b).

sional with many (five, six or seven) monolayers growing together at the same time (Fig. 8(b)), and the surface roughness Δ increases over time (Fig. 8(a)).

We have also studied the growth of silicon-like semiconductor structures with ridges formed on the top of a (411) surface with (111) side walls. A schematic representation of the structure grown at a substrate temperature $T = 700$ K is shown in Fig. 9. The deposition rate was 1 ML s^{-1}, the dimensions of substrate lattice were 20×40 with the x axis along [122], and the y axis along the [011] direction respectively. The result of this simulation is similar to that depicted in Fig. 6. The width of quantum wires formed on the (001) and (411) ridges is approximately the same. The difference is in the shape of these structures. While the quantum wire grown on the ridge on the (001) plane is symmetrical, the corresponding wire on the (411) ridge forms two different angles between (111) side walls and the (411) substrate.

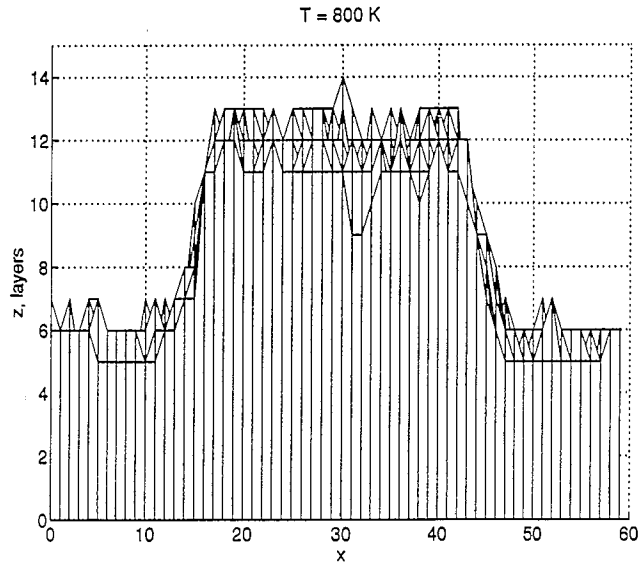

Fig. 7. The front view of the surface configuration after deposition of six additional monolayers of Si onto (30 × 80) lattice site area on a five-monolayer-thick (60 × 80) Si(001) buffer layer.

The (111) side walls are flat (owing to enhanced adatom migration on this surface at $T = 700$ K), and the (411) surface has a roughness which is comparable with Δ at $T = 700$ K of the (001) surface. Therefore, we do not observe a decrease in surface roughness for growth on the (411) plane.

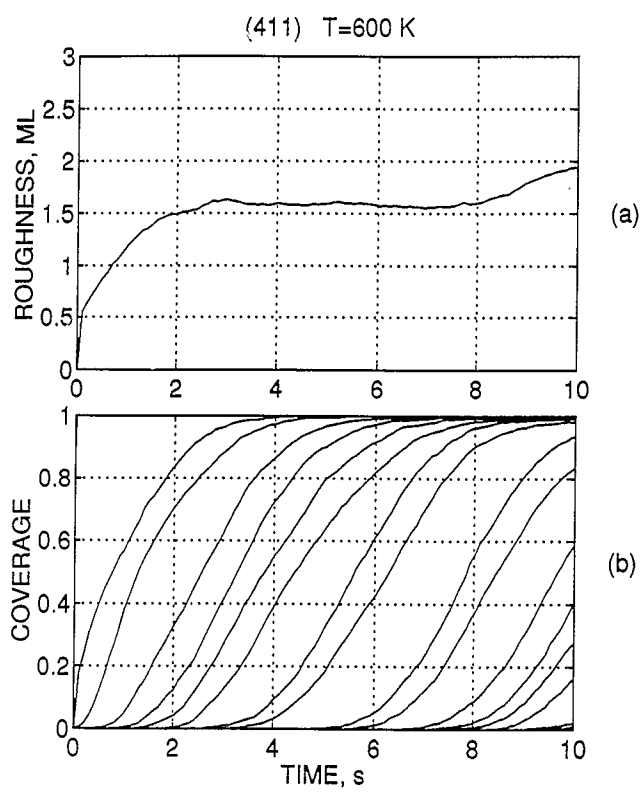

Fig. 8. Temporal evolution of the surface roughness (a), and filling of layers during deposition (b) of ten monolayers of silicon onto a (411) plane at $T = 600$ K.

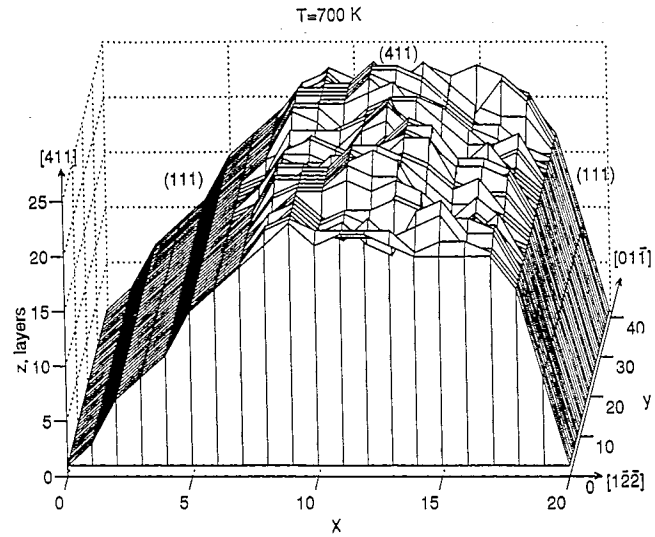

Fig. 9. Schematic representation of the structure with ridge formed on the top of a (411) surface with the (111) side walls grown at a substrate temperature $T = 700$ K.

References

[1] E. Kapon, M.C. Tamargo and D.M. Hwang, *Appl. Phys. Lett.*, *50* (1987) 347.

[2] H.P. Meier, E. Van Gieson, P.W. Gieson, P.W. Epperlein, C. Harder, W. Walter, M. Krahl and D. Bimberg, *J. Cryst. Growth*, *95* (1989) 66.

[3] E.M. Clausen, Jr., E. Kapon, M.C. Tamargo and D.M. Hwang, *Appl. Phys. Lett.*, *56* (1990) 776.

[4] S. Guha, A. Madhukar, K. Kaviani and R. Kapre, *J. Vac. Sci. Technol. B*, *8* (1990) 149.

[5] X.Q. Shen, M. Tanaka and T. Nishinaga, *J. Cryst. Growth*, *127* (1993) 932.

[7] M.E. Hoenk, H.Z. Chen, A. Yariv, H. Morkoc and K.J. Vahala, *Appl. Phys. Lett.*, *54* (1989) 1347.

[8] M.E. Hoenk, C.V. Nieh, H.Z. Chen and K.J. Vahala, *Appl. Phys. Lett.*, *55* (1989) 53.

[9] M. Hata, T. Isu, A. Watanabe and Y. Katayama, *J. Vac. Sci. Technol. B*, *8* (1990) 692.

[10] M. Hata, T. Isu, A. Watanabe and Y. Katayama, *Appl. Phys. Lett.*, *56* (1990) 2542.

[11] F.S. Turco, S. Simhony, K. Kash, D.M. Hwang, T.S. Ravi, E. Kapon and M.C. Tamargo, *J. Cryst. Growth*, *104* (1990) 766.

[12] T. Rohr, M. Walther, S. Rochus, G. Bohm, W. Klein, G. Trankle and G. Weimann, *Mater. Sci. Eng.*, *B21* (1993) 153.

[13] M. Walther, T. Rohr, G. Bohm, G. Trankle and G. Weimann, *J. Cryst. Growth*, *127* (1993) 1045.

[14] N. Haider, M.R. Wilby and D.D. Vvendensky, *Appl. Phys. Lett.*, *62* (1993) 3108.

[15] D.D. Vvedensky, N. Haider, T. Shitara and P. Smilauer, *Philos. Trans. R. Soc. London, Ser. A*, *344* (1993) 493.

[16] J.D. Weeks and G.H. Gilmer, *Adv. Chem. Phys.*, *40* (1979) 157.

[17] K.J. Hugill, S. Clarke, D.D. Vvedensky and B.A. Joyce, *J. Appl. Phys.*, *66* (1989) 3415.

[18] K.J. Hugill, T. Shitara, S. Clarke, D.D. Vvedensky and B.A. Joyce, *Mater. Res. Soc. Symp. Proc.*, *160* (1990) 405.

[19] S.A. Barnett and A. Rockett, *Surf. Sci.*, *198* (1988) 133.

[20] P.A. Maksym, *Semicond. Sci. Technol.*, *3* (1988) 594.

[21] M. Ichikawa and T. Doi, Appl. Phys. Lett., *50* (1987) 1141.

[22] E. Kasper, *Appl. Phys. A*, *28* (1982) 129.

[23] E. Kasper and J.C. Bean, *Silicon Molecular Beam Epitaxy*, CRC Press, Boca Raton, EL, 1988.

[24] T. Sakamoto, K. Sakamoto, K. Miki, H. Okumura, S. Yoshida and H. Tokumoto, in M.G. Lagally (ed.), *Kinetics of Ordering and Growth on Surfaces*, Plenum, New York, 1991, p. 263.
[25] J.M. McCoy, P.A. Maksym and T. Kawamura, *Suf. Sci.*, *257* (1991) 353.
[26] T. Sakamoto, N.J. Kawai, T. Nakagawa, K. Ohta and T. Kojima, *Appl. Phys. Lett.*, *47* (1985) 617.
[27] J. Aarts and P.K. Larsen, *Surf. Sci.*, *188* (1987) 391.
[28] T. Yokotsuka, M.R. Wilby, D.D. Vvedensky, T. Kawamura, K. Fukutani and S. Ino, *Appl. Phys. Lett.*, *62* (1993) 1673.
[29] J. Brunner, T.S. Rupp, H. Gossner, R. Ritter, I. Eisele and G. Abstreiter, *Appl. Phys. Lett.*, *64* (1994) 994.
[30] J. Gondermann, B. Spangenberg, T. Koster, B. Hadam, H.G. Roskos, H. Kurz, J. Brunner, P. Schittenhelm, G. Abstreiter, H. Gossner and I. Eisele, *Microelectron. Eng.*, *27* (1995) 83.
[31] J. Brunner, P. Schittenhelm, J. Gondermann, B. Spangenberg, B. Hadam, T. Koster, H.G. Roskos, H. Kurz, H. Gossner, I. Eisele and G. Abstreiter, *J. Cryst. Growth*, *150* (1995) 1060.
[32] S. Shimomura, S. Ohkubo, Y. Yuba, S. Namba, S. Hiyamizu, M. Shigeta, T. Yamamoto and K. Kobayashi, *Surf. Sci.*, *267* (1992) 13.